Fabrication and Characterization of a Hierarchical Manifold Microchannel Heat Sink Array for Evaporative Intrachip Cooling

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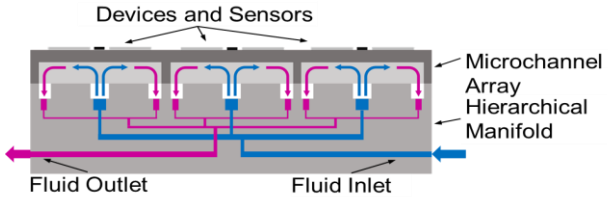
Objective

Design, fabricate, and characterize a hierarchical manifold microchannel heat sink to dissipate high heat fluxes at low pressure drops using evaporative cooling.

Approach

- Deliver HFE-7100 to a 9 × 9 array of silicon microchannel heat sinks via a hierarchical manifold distributor.
- Parallel flow paths allow for shorter flow lengths and decreased pressure drop.
- Scalable design allows for further flow discretization.

Schematic Diagram of Heat Sink Concept



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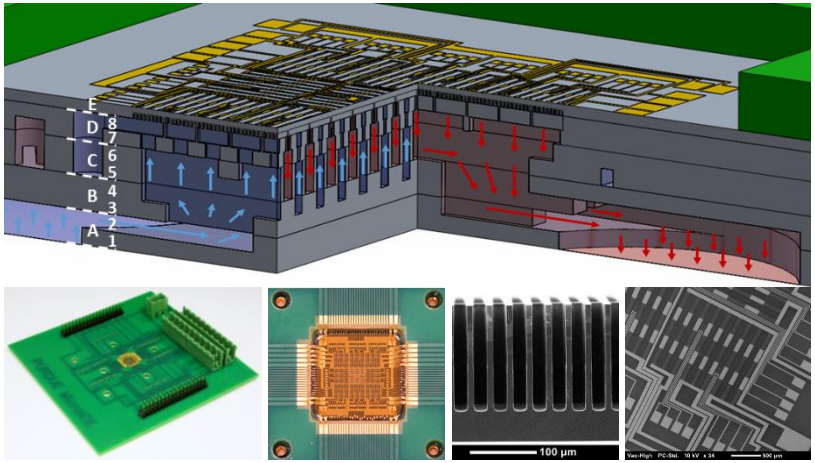
Test Vehicle, Wire-Bonded Chip, Channel Cross-Sections, and Heaters/RTDs



Results

- Dissipated high heat fluxes (~ 450 W/cm²) at reasonable pressure drops (< 75 kPa) and low chip temperature rise (< 30 ° C).
- Low mass flux needed for high performance.
- Increasing fluid mass flux increases maximum heat flux.
- Maximum heat transfer coefficient occurs at intermediate heat flux.

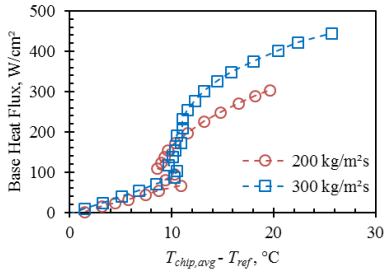
Selected Publications

- K. P. Drummond, J. A. Weibel, S. V. Garimella, D. Back, D. B. Janes, M. D. Sinanis, and D. Peroulis, 40th GOMACTech Conference, 2015.
- K. P. Drummond, J. A. Weibel, S. V. Garimella, D. Back, D. B. Janes, M. D. Sinanis, and D. Peroulis, ITHERM Conference, 2016.

Fabrication

- Etch high aspect-ratio microchannels into silicon (DRIE).
- Pattern heaters and an array of RTDs on backside of microchannels to apply heat flux and measure chip temperatures, respectively.
- Fabricate hierarchical manifold to facilitate fluid delivery to microchannel array.
- Bond manifold to microchannels

Heat Flux vs. Chip Temp



Heat Trans. Coeff. vs. Flux