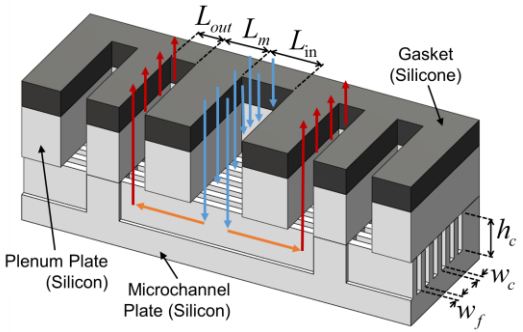
Fabrication and Characterization of a Hierarchical Manifold Microchannel Heat Sink Array for Evaporative Intrachip Cooling

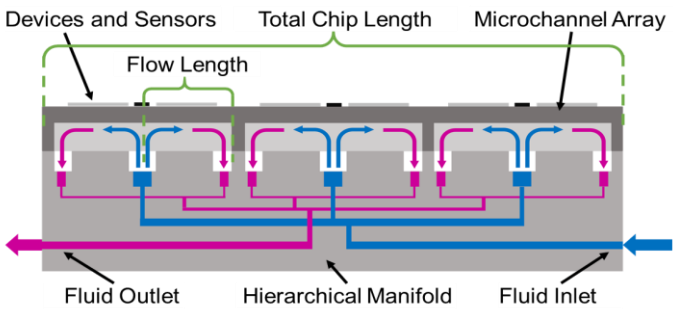
K. P. Drummond, J. A. Weibel, S. V. Garimella, D. Back, D. B. Janes, M. D. Sinanis, and D. Peroulis

Objective

Design, fabricate, and characterize a hierarchical manifold microchannel heat sink to dissipate high heat fluxes at low pressure drops using evaporative cooling.



Schematic diagram of the heat sink unit cell showing the fluid flow paths



Cross-sectional schematic diagram of the manifold microchannel heat sink design concept in the current work.

Approach

- Deliver HFE-7100 working fluid to a 3 × 3 array of silicon microchannel heat sinks via hierarchical manifold distributor.
- Parallel flow paths allows for shorter flow lengths and thus decreased pressure drop.
- Scalable design will allow for further flow discretization in the future

PURDUE UNIVERSITY DARPA IceCool

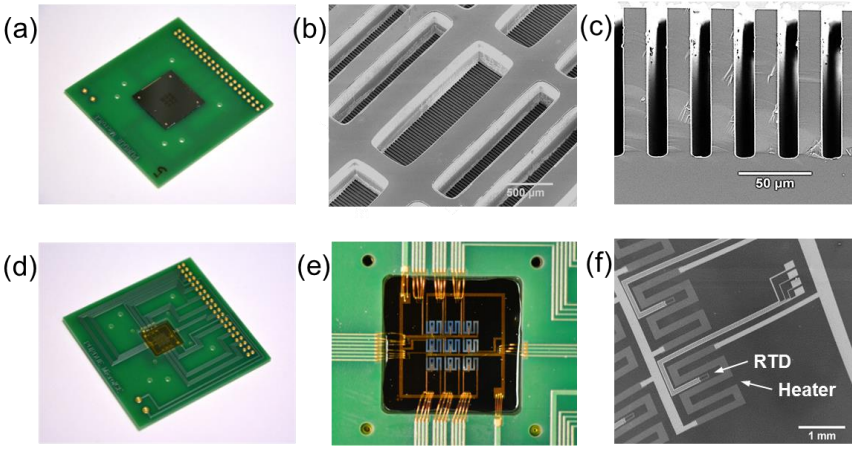
This work is supported by the DARPA Intrachip/ Interchip Enhanced Cooling (ICECool) Fundamentals program, conceived and led by Dr. Avram Bar-Cohen.

Selected Publications

- K. P. Drummond, J. A. Weibel, S. V. Garimella, D. Back, D. B. Janes, M. D. Sinanis, and D. Peroulis, 40th Government Microcircuit Applications and Critical Technology Conference (GOMACTech), 2015.
- S. Sarangi, K. K. Bodla, S. V. Garimella, J. Y. Murthy, *Int. J. Heat and Mass Transfer*, Vol. 69, 92-105, 2014

Design and Fabrication

- Etch high aspect-ratio microchannels (15 μm × 255 μm; AR = 17) into silicon chip using DRIE.
- Pattern heaters and an array of 4-wire RTDs on backside of microchannels to apply heat flux and measure chip temperatures, respectively.
- Wire-bond on-chip electrical connections to PCB for convenient, reliable interface.
- Fabricate hierarchical manifold distributor using high-resolution stereolithography to facilitate fluid delivery to microchannel array.



(a) Photograph of the test chip with channels face up, (b) SEM image of plenum plate, (c) cross-sectional SEM image of the microchannels, (d) photograph of heater and sensors, (e) heater and sensors wire-bonded to PCB, and (f) SEM image of serpentine heaters, RTDs, and lead-wires.