Hackathon @ Chips & AI Workshop

Key Dates

Registration opens	**Aug 24, 2026**
Proposal due / registration closes	**Sep 6, 2026**
Final submission	**Sep 19, 2026**
Finalists notified	**Sep 21, 2026**
Demos and awards	**Sep 22, 2026, at the workshop**

Overview

The Chips & AI Hackathon is an open-ended challenge focused on ideas at the intersection of artificial intelligence and semiconductor hardware. Participants identify a meaningful problem and develop a prototype, model, simulation, circuit concept, or proof of concept.

The hackathon concludes at the Chips & AI Workshop, allowing selected participants and teams to demonstrate their technical skills, share their work with faculty and industry participants, and build connections with researchers and professionals working across AI, semiconductor design, and computing systems.

The suggested themes are starting points rather than rigid tracks. Cross-theme and related project ideas are welcome.

Eligibility and Teams

- Undergraduate students, graduate students, and postdoctoral researchers from across Purdue University are eligible.
- Participants may compete solo or in teams of 2–4.
- Teams may be formed before registration or during the first week.
- Cross-department teams are encouraged.
- Expertise in either AI or hardware is recommended; expertise in both is not necessary.

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Suggested Themes

1. Algorithmic Efficiency & Inference Acceleration

Develop faster and more memory-efficient AI models and serving algorithms.

- **Inference acceleration algorithms:** Speculative decoding, early exiting, and efficient attention mechanisms (e.g., FlashAttention, Mamba/SSMs).
- **Memory optimization:** KV-cache management, paging, and context-window compression.
- **Model compression:** Quantization (e.g., FP8, INT4), pruning, and sparsity.
- **Hardware-aware optimization:** Knowledge distillation and neural architecture search (NAS) optimized for specific chip constraints.

2. Agentic Architectures & System-Level AI

Design architectures, frameworks, and pipelines for autonomous agents and multi-agent systems.

- **Hardware-software co-design for agents:** Optimizing hardware allocation for agents that rapidly switch between reasoning, tool use, and generation.
- **Efficient RAG & memory:** Accelerating Retrieval-Augmented Generation pipelines and long-term agentic memory architectures.
- **Edge agents:** Lightweight frameworks for deploying autonomous, tool-calling agents on local devices, mobile NPUs, or embedded systems.
- **Multi-agent orchestration:** Efficient scheduling and compute routing for complex multi-agent workflows and continuous learning systems.

3. AI Hardware Accelerators

Design hardware, dataflows, or heterogeneous systems optimized for modern AI training and inference.

- **Accelerator architectures:** Custom dataflows, spatial accelerators, and systolic arrays.
- **Memory-hierarchy optimization:** Overcoming the memory wall for large language models (LLMs) and transformer architectures.
- **Compute acceleration:** Novel architectures for attention mechanisms, matrix multiplication, and vector processing.
- **Heterogeneous systems:** Coordinated mapping across CPU, GPU, NPU, and FPGA environments.

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4. In-Memory Computing and Circuits

Explore circuits and physical architectures that fundamentally reduce the cost of data movement.

- **In-Memory Computing (IMC):** Analog or digital IMC macro designs and mixed-signal AI circuits.
- **Compute-near-memory:** Near-data processing architectures (e.g., processing inside HBM or 3D-stacked memory).
- **Novel primitives:** Utilizing emerging memory technologies (ReRAM, PCM, MRAM) for synaptic weights.
- **Simulation & mapping:** Tools and compilers for mapping neural networks onto non-traditional analog/mixed-signal hardware.

5. Machine Learning for EDA (AI for Chips)

Apply machine learning to improve, automate, or accelerate the chip-design workflow.

- **Physical design:** AI-driven floorplanning, placement, and routing optimization.
- **Predictive modeling:** Machine learning for rapid timing, power, thermal, or area estimation before final synthesis.
- **Verification:** AI agents for automated debugging, testbench generation, or formal verification.
- **Design-space exploration:** Reinforcement learning or Bayesian optimization for architectural tuning and parameter search.

Cross-Theme and Open Projects

Projects do not need to fit neatly within one suggested theme. Any idea with a meaningful connection to AI and semiconductor hardware is welcome.

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Hackathon Timeline

Aug 24–Sep 6 — Register, Form Teams, and Propose

- Registration opens Aug 24. Participants may register individually or as a team, refine their project idea, and submit a one-page proposal through the registration form by Sep 6. Registration closes with the proposal deadline.

Sep 7–13 — Build and Iterate

- Implement and test the core idea, refine the project scope based on early results and technical constraints, and document key decisions and progress.

Sep 14–19 — Finalize and Submit

- Complete the implementation or proof of concept, run appropriate experiments, simulations, or benchmarks, and submit the final demo video by Sep 19.

Sep 21 — Finalists Announced

- Selected participants and teams will be notified and invited to demonstrate their projects at the workshop.

Sep 22 — Final Showcase and Awards

- Finalists will get a chance to network and demonstrate their projects to the faculty and industry partners in attendance during the Chips & AI Workshop. Judges will decide the winners and the awards will be presented during the Workshop.

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Required Deliverables

One-Page Proposal

The one-page proposal is due Sep 6, 2026, and should be submitted through the registration form. Keep it to one page and use it to clearly communicate the project you intend to pursue. Include the problem and motivation, your proposed technical approach, the relevant suggested theme(s) or cross-theme connection, the prototype/model/simulation/circuit/proof of concept you expect to build, and how you plan to evaluate or demonstrate success. Early-stage ideas are welcome—the proposal is intended to establish a clear technical direction, not require completed results. Register and submit the proposal here: https://forms.cloud.microsoft/r/SFZyWs6KCg

Demo Video

The final submission consists of a single, concise recorded demo video that communicates the project's core idea, technical approach, and key results. No code repository, written report, or separate presentation is required.

Final Showcase

Selected participants and teams will be invited to the final showcase, where they will demonstrate their projects during the workshop. A formal presentation is not required.

Judging Criteria

Criterion	Weight
Technical Merit and Innovation	30%
Relevance to AI and Chips	20%
Results and Evidence	20%
Implementation Quality	20%
Demo Video Clarity	10%

Projects will be judged on the strength of the idea and evidence of execution, not simply on scale or complexity. Software, models, RTL, simulations, circuits, and hardware prototypes are all welcome.

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Awards

Outstanding projects will be recognized during the workshop. Awards will highlight projects that demonstrate exceptional technical merit, innovation, relevance to AI and semiconductor hardware, strong evidence of execution, and clear communication. Multiple projects may be recognized, with final award categories and prize details announced separately.

How to Participate

- ***Registration and proposal submission:***

  https://forms.cloud.microsoft/r/SFZyWs6KCg

- ***Questions:*** ***chipsAIHackathon@purdue.edu***

Build something meaningful, measure what you can, and show what you learned.