Effects of $(NH_4)_2S$ passivation on the off-state performance of 3-dimensional InGaAs metal-oxide-semiconductor field-effect transistors

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Planar and 3-dimensional (3D) buried-channel InGaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) have been experimentally demonstrated at deep-submicron gate lengths. The effect of $(NH_4)_2S$ passivation with different concentrations (20%, 10%, or 5%) on the off-state performance of these devices has been systematically studied. 10% $(NH_4)_2S$ treatment is found to yield the optimized high-k/InP barrier layer interface property, resulting in a minimum subthreshold swing (SS) lower than 100 mV/dec. Moreover, the 3D device structure greatly improves the off-state performance and facilitates enhancement-mode operation. A scaling metrics study has been carried out for 10% $(NH_4)_2S$ treated 3D devices with gate lengths down to 100 nm. With the optimized interface passivation, 3D III-V MOSFETs are very promising for future high-speed low-power logic applications. © *2011 American Institute of Physics*. [doi:10.1063/1.3651754]

Recently, surface-channel and buried-channel III-V metal-oxide-semiconductor field-effect transistors (MOSFETs) have been extensively studied for beyond 14 nm logic applications. Thanks to the continuous progress on improving high-k/III-V interfaces, inversion-mode InGaAs MOSFETs with high drive current have been realized with various gate stacks.[1–5] On the other hand, buried-channel InGaAs MOSFETs with GaAs/AlGaAs, InAlAs, or InP barrier[6–9] and quantum-well FETs (QWFETs) with thin InP barrier[10] have been shown to offer higher transconductance (g_m), higher effective mobility, and lower subthreshold swing (SS) compared to surface-channel III-V MOSFETs. Furthermore, nonplanar structure has recently been introduced to III-V device fabrication to suppress short channel effects (SCEs) at deep-submicron gate lengths. Much better off-state performance has been obtained on InGaAs FinFETs (Refs. 11 and 12) and multi-gate QWFETs (Ref. 13). Therefore, a 3-dimensional (3D) buried-channel InGaAs MOSFET is promising candidate for ultimately scaled III-V device technology. $(NH_4)_2S$ passivation is a common pre-gate treatment to improve the interface quality of III-V MOSFETs. O'Connor *et al.* recently reported a systematic Al_2O_3/InGaAs interface study with different $(NH_4)_2S$ passivation conditions.[14] Superior capacitance-voltage (CV) characteristics have been achieved on 10% $(NH_4)_2S$ treated samples. However, the impact of different sulfur passivation conditions on the interface property of InGaAs MOSFETs at the device level is lacking. In a buried-channel InGaAs MOSFET, although the oxide/semiconductor interface is not directly located at the high mobility channel, the high-*k*/barrier layer interface is of great importance to achieve good off-state performance of the device and, therefore, it can also be a good test vehicle for optimization of the sulfur passivation.

In this letter, we fabricated planar and 3D buried-channel InGaAs MOSFETs and systematically study the effect of $(NH_4)_2S$ passivation with different concentrations (20%, 10%, or 5%) on the off-state performance of the devices. It is found that 10% $(NH_4)_2S$ passivated devices show the best interface property, yielding a lower SS and drain-induced barrier lowering (DIBL). The positive threshold voltage (V_T) shift of the 20% and 5% $(NH_4)_2S$ treated devices confirms that more acceptor traps remain unpassivated in these devices. Moreover, a detailed scaling metrics study of 3D buried-channel InGaAs MOSFETs treated with 10% $(NH_4)_2S$ is also carried out for gate length (L_G) down to 100 nm. By implementing 3D structure, a SS lower than 100 mV/dec has been obtained and enhancement-mode operation is achieved.

MOSFET fabrication started with a 2 in. semi-insulating InP substrate. A 300 nm undoped $In_{0.52}Al_{0.48}As$ buffer layer, 10 nm undoped $In_{0.7}Ga_{0.3}As$ channel layer, 2 nm undoped InP barrier layer, and 20 nm N+ doped InGaAs layer were sequentially grown by molecular beam epitaxy. Device

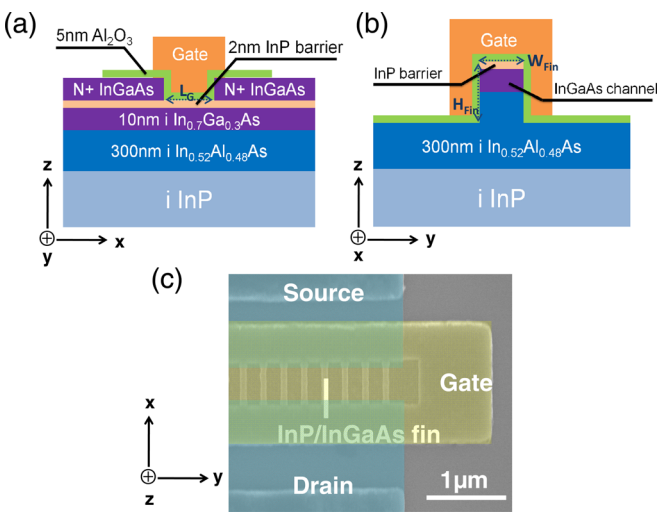

FIG. 1. (Color online) (a) Schematic diagram of planar and 3D buried-channel InGaAs MOSFETs in x-z plane, (b) Cross sectional view of 3D buried-channel InGaAs MOSFETs in y-z plane, and (c) Top-view SEM image of a finished 3D buried-channel InGaAs MOSFET with $W_{fin} = 30$ nm and $L_G = 350$ nm.

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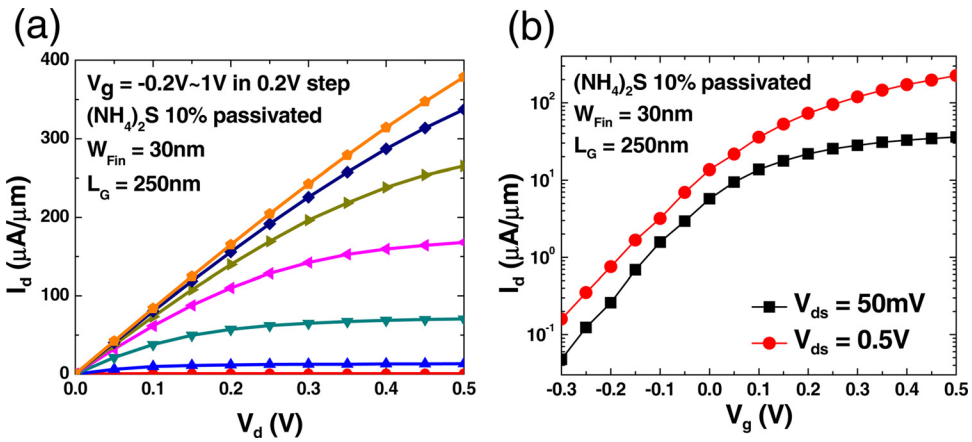

FIG. 2. (Color online) (a) Output and (b) transfer characteristics of a typical 3D buried-channel InGaAs MOSFET with $L_G = 250$ nm, $W_{Fin} = 30$ nm, and passivated by 10% $(NH_4)_2S$.

isolation and gate recess etching were then performed using citric acid based solution. The gate lengths of the devices were varied from 0.5 μm down to 100 nm. For non-planar devices, a fin etching process was done using BCl_3/Ar based reactive ion etching.[11] The smallest fin width (W_{Fin}) defined was 30 nm and the fin height (H_{Fin}) was around 50 nm. After short buffered oxide etch (BOE) dip, the samples were soaked in $(NH_4)_2S$ (20%, 10%, or 5% diluted in H_2O). The passivation time was fixed at 10 min for all three $(NH_4)_2S$ concentrations in this experiment. The passivation time of 10 min is optimized by the detailed Al_2O_3/InP capacitance-voltage interface studies. The air exposure after sulfur treatment was minimized. The samples were then loaded into an ASM F-120 atomic-layer deposition (ALD) reactor for 5 nm Al_2O_3 deposition at 300 °C. Source/drain contacts were then formed by Au/Ge/Ni deposition and 350 °C rapid thermal annealing process (RTA). Finally, Ni/Au was electron beam evaporated as gate metal. Since sulfur passivation was found to be unstable after thermal treatment higher than 400 °C,[15] no post deposition annealing (PDA) was performed after ALD gate dielectric deposition, and the thermal budget of the entire fabrication process was as low as 350 °C. All patterns were defined by a Vistec UHR electron beam lithography system.

Figure 1(a) shows the schematic diagram of the planar and 3D buried-channel InGaAs MOSFETs fabricated in this work. Figure 1(b) shows the schematic cross section in y-z plane for 3D devices. A top view scanning electron microscopy (SEM) image of a finished device with parallel fin structures is shown in Figure 1(c). Figures 2(a) and 2(b) show the well-behaved output and transfer characteristics of a 3D buried-channel InGaAs MOSFET with $L_G = 250$ nm, $W_{Fin} = 30$ nm and passivated with 10% $(NH_4)_2S$ before gate oxide deposition. A saturation drain current of 380 μA/μm and g_m of 557 μS/μm is obtained at $V_{ds} = 0.5$ V. The threshold voltage (V_T) of the device is −0.05 V from linear extrapolation at $V_{ds} = 50$ mV and −0.18 V using 1 μA/μm metric at $V_{ds} = 0.5$ V. A SS of 120 mV/dec and DIBL of 99 mV/V are also achieved. Compared to deep-submicron surface-channel InGaAs MOSFETs, a higher g_m is obtained at a lower drain voltage with the same gate oxide thickness,[16] indicating the advantage of buried-channel devices for low-voltage operation.

To study the effect of different sulfur passivation conditions, the SS and V_T of planar and 3D devices with $(NH_4)_2S$ (20%, 10%, or 5%) passivation are shown in Figures 3(a) and 3(b), respectively. To minimize the influence from the SCE, $L_G = 0.5$ μm devices are investigated. First, the 10% $(NH_4)_2S$ treated devices show the lowest SS of 96 mV/dec, indicating a lower interface trap density (D_{it}) at the Al_2O_3/InP barrier layer interface. The upper limit of midgap D_{it} is estimated to be around 4.6×10^{12}/eV·cm^2 for 10% $(NH_4)_2S$ treated surface. The reduction of D_{it} indicates the effective suppression of native oxides at high-k/InP interface by 10% $(NH_4)_2S$ passivation, being evident from the lack of In^{3+} states detected in Al_2O_3/InP (100) x-ray photoelectron spectroscopy (XPS) characterization. This is in good agreement with the previous XPS study on high-k/InGaAs interface, where lowest amount of surface oxides are present in 10% $(NH_4)_2S$ treated samples.[17] However, SS values alone cannot distinguish between acceptor/donor traps.[18] Second, 10% $(NH_4)_2S$ treated devices show lower V_T than 20% or 5% $(NH_4)_2S$ treated devices. This indicates that 20% and 5% $(NH_4)_2S$ treatment is less effective in passivating acceptor traps, resulting in a positive V_T shift. Moreover, the highest drain current is also obtained on 10% $(NH_4)_2S$ passivated devices at the same gate voltage overdrive (V_G–V_T). This again suggests that the unpassivated surface traps are mostly acceptor-like. These observations are consistent with the conclusion from previous interface study on surface-channel InGaAs MOSFETs,[18] where simulation results show that acceptor-like traps degrade SS, V_T, and on-current. It is also noted that similar results have been found on Ge surface and interfaces, where unpassivated acceptor defects delays inversion in Ge nMOSFETs.[19] Third, the DIBL of 10% $(NH_4)_2S$ passivated devices are also found to be the lowest. This may result from a better gate electrostatic control of the channel,

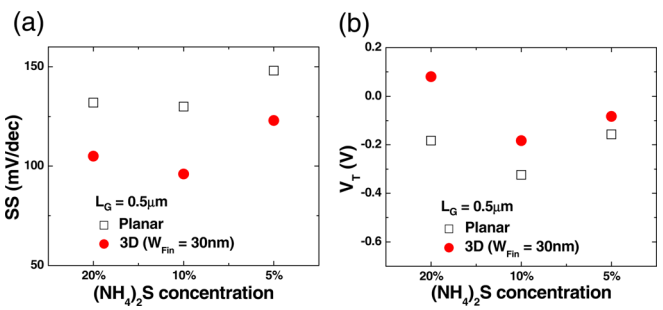

FIG. 3. (Color online) (a) SS and (b) V_T of planar and 3D ($W_{Fin} = 30$ nm) buried-channel InGaAs MOSFETs ($L_G = 0.5$ μm) with 20%, 10%, or 5% $(NH_4)_2S$ passivation. V_T is determined by 1 μA/μm metric at $V_{ds} = 0.5$ V.

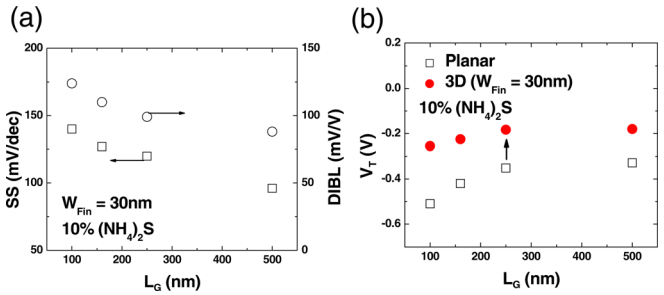

FIG. 4. (Color online) (a) SS and DIBL versus L_G of 3D ($W_{Fin} = 30$ nm) buried-channel InGaAs MOSFETs and passivated with 10% $(NH_4)_2S$ (b) V_T versus L_G of planar and 3D ($W_{Fin} = 30$ nm) buried-channel InGaAs MOSFETs passivated with 10% $(NH_4)_2S$. V_T is determined by 1 μA/μm metric at $V_{ds} = 0.5$ V.

due to the better gate oxide/barrier layer interface quality. Although not a direct effect of D_{it}, a lower DIBL is desired when device dimension scales down to deep-submicron regime. Finally, the 3D devices with $W_{Fin} = 30$ nm show lower SS and increase in V_T, compared to the planar devices. By introducing 3D structure, the devices can be switched off faster and enhancement-mode operation can be more easily achieved. In summary, 10% $(NH_4)_2S$ passivation is found to yield the best interface quality and optimum off-state performance for planar and 3D buried-channel InGaAs MOSFETs.

Furthermore, we investigate the scaling metrics of the buried-channel InGaAs MOSFETs with 10% $(NH_4)_2S$ passivation and the gate lengths of the devices varied from 0.5 μm down to 100 nm. Figure 4(a) shows the SS and DIBL versus L_G for non-planar devices with $W_{Fin} = 30$ nm, where SS is obtained at a drain voltage of 0.5 V. It is found that SS and DIBL gradually increase with L_G shrinking due to the SCE. Further suppression of SCE can be achieved by reducing W_{Fin},[11] decreasing the equivalent oxide thickness, or implementing more advanced 3D structure such as gate-all-around structure.[20] Figure 4(b) shows the V_T versus L_G for planar and 3D devices with $W_{Fin} = 30$ nm. A 0.15 V to 0.25 V positive V_T shift has been observed for 3D devices, making the device operation more approaching enhancement-mode. Moreover, 3D devices show better threshold roll-off property due to a better electrostatic control of the channel. These results highlight the importance of introducing advanced 3D structure to the fabrication of III-V MOSFETs at deep submicron gate lengths.

In conclusion, planar and 3D buried-channel InGaAs MOSFETs have been demonstrated with gate length down to 100 nm. The effects of sulfur passivation with different $(NH_4)_2S$ concentrations (20%, 10%, or 5%) on the off-state performance of the planar and 3D devices are systematically studied. It is found that 10% $(NH_4)_2S$ is the optimum sulfur passivation condition, resulting in a better Al_2O_3/InP barrier layer interface. A scaling metrics study of the 3D buried-channel InGaAs MOSFETs is also carried out and the benefits of 3D structures are confirmed with lower SS, DIBL, and higher V_T, making 3D III-V MOSFETs very promising for beyond 14 nm logic applications. The optimized sulfur passivation technique is applicable to the fabrication of surface-channel InGaAs MOSFETs as wells as bottom-up GaAs, InGaAs, and InAs nanowire FETs,[21,22] providing a simple solution to improve high-k/III-V interface quality.

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