First Demonstration of Top-Gate Enhancement-Mode ALD In_2O_3 FETs with High Thermal Budget of 600 °C for DRAM Applications

Jian-Yu Lin†, Zhuocheng Zhang†, Zehao Lin, Chang Niu, Yizhi Zhang, Yifan Zhang, Taehyun Kim, H. Jang, C. Sung, M. Hong, S. M. Lee, T. Lee, M. H. Cho, D. Ha, Changwook Jeong, Haiyan Wang, M. A. Alam, *Fellow, IEEE*, and Peide D. Ye*, Fellow, IEEE*

Abstract— **In this work, for the first time, we report top-gate In_2O_3 FETs with enhancement-mode (E-mode) operation and a high thermal budget of 600 °C, being compatible with dynamic random-access memory (DRAM) fabrication which requires high-temperature processes (> 550 °C). The robustness of In_2O_3 channel under high-temperature treatment is confirmed by transmission electron microscope (TEM) and good electrical characteristics of drain current of 350 μA/μm (at V_{DS} = 2 V), threshold voltage (V_T) ~ 1 V, and low off-current ~ 10^{-14} A/μm determined by measurement detection limit in scaled devices with a channel length of 100 nm. Reliability characteristics of the devices are found to change with different process temperatures and can be explained by the proposed trap distribution model at the dielectric/In_2O_3 interface. This research indicates that top-gate E-mode In_2O_3 FETs with high-thermal budget and ultra-low off-current could find their promise to replace single crystal silicon channel for next-generation DRAM technology.**

Index Terms— **Atomic Layer Deposition (ALD), indium oxide, enhancement-mode, high thermal budget, DRAM.**

I. Introduction

OXIDE semiconductor channel transistors, like InGaZnO FETs, have been considered as the candidate for next-generation dynamic random-access memory (DRAM) devices due to their ultralow off-current (I_{off} ~10^{-21} A/μm), which can significantly suppress the leakage current and extend the retention time in DRAM [1-2]. Besides low I_{off}, enhancement-mode (E-mode) devices with top-gate structure and compatibility with high-temperature (> 550 °C) processes during DRAM fabrication are two other crucial requirements for oxide FETs in DRAM applications [3-4]. Although many works have demonstrated oxide channel FETs with E-mode and top-gate structure, they all focus on the devices fabricated at low-temperature (< 400 °C) for back-end-of-line monolithic 3D integration [5-8]. Under the condition of high thermal budget process (> 550 °C) compatibility, no oxide semiconductor channel transistor with E-mode operation and top-gate structure has been reported yet.

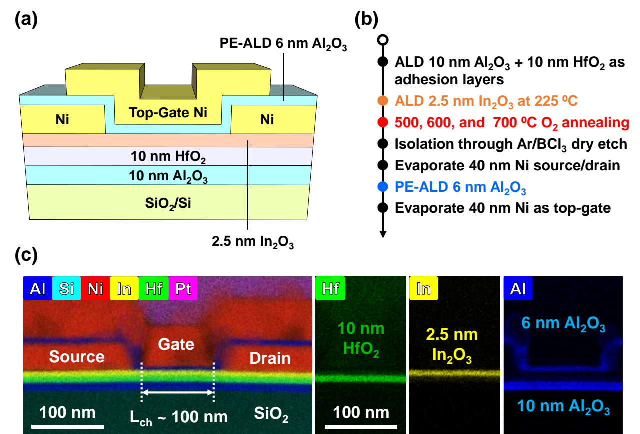

Fig. 1. (a) Device schematic and (b) fabrication process flow of top-gate In_2O_3 FETs with high-temperature (500 – 700 °C) O_2 annealing. (c) Cross-sectional TEM and EDX mappings (Hf, In, and Al) of an In_2O_3 FET with L_{ch} = 100 nm and 600 °C O_2 annealing. The robustness of the In_2O_3 film after 600 °C process can be confirmed.

In this work, we demonstrate the first top-gate In_2O_3 FETs, one of the well-studied oxide semiconductor transistors, with threshold voltage (V_T) ~ 1 V (E-mode), channel length (L_{ch}) of 100 nm, good drain current (I_D) of 350 μA/μm (at V_{DS} = 2 V), low I_{off} ~10^{-14} A/μm determined by the measurement setup detection limit, and O_2 annealing process with high thermal budget of 600 °C on the channel. This research demonstrates great potential of top-gate E-mode In_2O_3 transistors with high thermal budget compatibility for future DRAM applications.

II. Experiments

Fig. 1 (a) illustrates the device schematic of a top-gate In_2O_3 FET. The fabrication process started with the deposition of 10 nm Al_2O_3 at 175 °C and 10 nm HfO_2 at 200 °C by ALD on SiO_2/Si substrate as the bottom adhesion layers. Then, 2.5 nm In_2O_3 was grown by ALD at 225 °C, followed by high-

The work is supported by Samsung Electronics and Air Force Office of Scientific Research (AFOSR). †Equally contributing authors.

Jian-Yu Lin, Zhuocheng Zhang, Zehao Lin, Chang Niu, M. A. Alam, and Peide D. Ye are with the Elmore Family School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

Yizhi Zhang, Yifan Zhang, and Haiyan Wang are with the School of Materials Science and Engineering, Purdue University, West Lafayette, IN 47907 USA.

Taehyun Kim and Changwook Jeong are with Graduate School of Semiconductor Materials and Devices Engineering, Ulsan National Institute of Science and Technology, Ulsan, Republic of Korea.

H. Jang is with Materials Science and Engineering, Ulsan National Institute of Science and Technology, Ulsan, Republic of Korea.

C. Sung, M. Hong, S. M. Lee, T. Lee, M. H. Cho, and D. Ha are with Advanced Device Research Lab, Semiconductor R&D Center, Samsung Electronics Co., Hwasung, Republic of Korea.

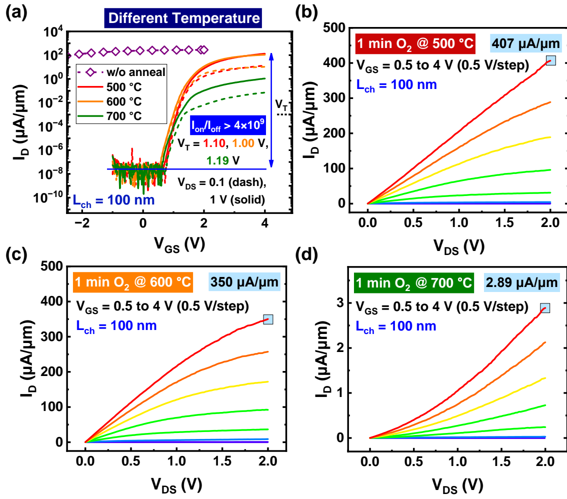

Fig. 2. (a) $I_D - V_{GS}$ curves of short-channel (L_{ch} = 100 nm) In_2O_3 FETs with different O_2 annealing conditions. In this work, V_T is extracted using constant drain current method at V_{GS} @ I_{DS} = 100 pA × W_{ch}/L_{ch}. Output characteristics of the In_2O_3 FETs with different O_2 annealing temperatures of (b) 500, (c) 600, and (d) 700 °C, respectively.

temperature O_2 annealing at 500, 600, and 700 °C for 1 minute, respectively. Next, channel isolation was performed by Ar/BCl_3 dry etching. 40 nm Ni was deposited by e-beam evaporation as source and drain. As for the gate dielectric, 6 nm of Al_2O_3 was grown by plasma-enhanced ALD (PE-ALD) using O_2 plasma as the precursor of oxygen to suppress the generation of oxygen vacancies (V_O) in oxide semiconductor channels during the dielectric deposition process [9]. Finally, 40 nm Ni was e-beam evaporated as top-gate. **Fig. 1 (b)** summarizes the fabrication process flow. All metallization process steps were performed after the high-temperature O_2 annealing to avoid damaging metal contacts. Transmission electron microscope (TEM) and energy dispersive X-ray (EDX) images of an In_2O_3 FET with 600 °C annealing are shown in **Fig. 1 (c)**. The TEM results indicate that In_2O_3 is a robust material that can survive after 600 °C process, which verifies the compatibility of In_2O_3 FETs with high thermal budget (> 550 °C) process in DRAM development.

III. Results and Discussions

Fig. 2 (a) presents the I_D-V_{GS} characteristics of the top-gate In_2O_3 FETs with a short channel length (L_{ch}) of 100 nm and various O_2 annealing conditions. It should be noted that all the short-channel devices demonstrate E-mode behavior with V_T = 1.10, 1.00, and 1.19 V for 500, 600, and 700 °C annealed FETs, respectively. On the other hand, w/o annealing device cannot be fully turned off and possess V_T < 0 V, which highlights the importance of O_2 annealing to achieve E-mode In_2O_3 devices. In addition to the E-mode, the I_{off} of these transistors are all close to the detection limit (~10^{-14} A/μm) of the semiconductor analyzer. Besides transfer characteristics, output characteristics of top-gate In_2O_3 FETs with different process temperatures are also studied and shown in **Fig. 2 (b – d)**. As the annealing temperature increases from 500 to 600 °C, the maximum drain current slightly decreases but remains a high drain current of 350 μA/μm at V_{DS} of 2 V for the 600 °C device, as illustrated in **Fig. 2 (b)** and **(c)**. **Fig. 3 (a)** exhibits the extracted V_T from the devices with different L_{ch} (1 μm – 100 nm) and annealing

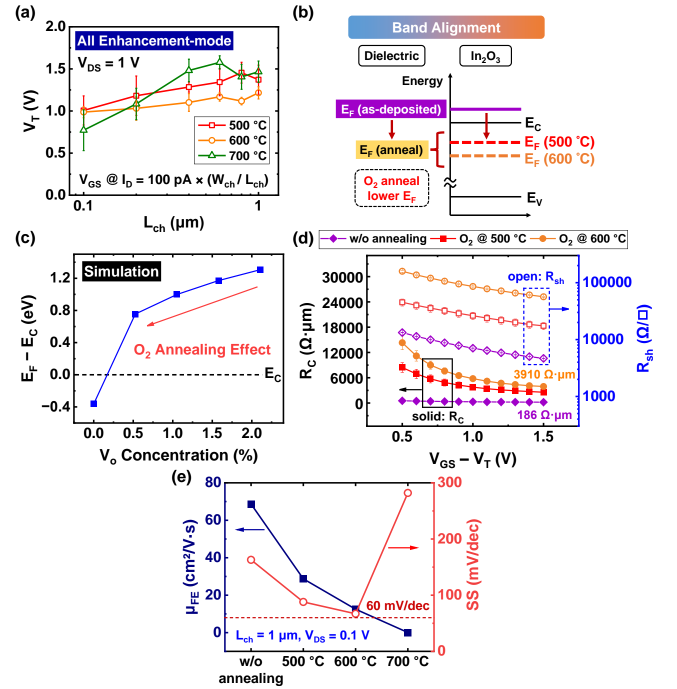

Fig. 3. (a) Extracted V_T from In_2O_3 FETs with different annealing temperatures as a function of L_{ch}. (b) Schematic band alignment at gate dielectric (Al_2O_3) /In_2O_3 interface. (c) First-principles simulated E_F position, relative to conduction band minimum (E_C), as a function of V_O concentration. (d) Extracted contact resistance (R_C) and sheet resistance (R_{sh}) by transfer length method (TLM). (e) Extracted field-effect mobility (μ_{FE}) and subthreshold swing (SS) from In_2O_3 FETs with different annealing conditions. μ_{FE} were extracted from the transconductance (g_m) of In_2O_3 FETs using measured gate oxide capacitance (C_{OX}) of 1 × 10^{-6} F/cm². Note that the extracted μ_{FE} do not exclude the effect of R_C and thus are underestimated values.

temperatures. All top-gate In_2O_3 FETs have V_T > 0 V. This is the first time E-mode In_2O_3 transistors with *top-gate structure* are demonstrated [10-11]. The main determinants of E-mode operation can be attributed to the high-temperature O_2 annealing and the PE-ALD dielectric formation process based on O_2 plasma [9]. 500-700 °C O_2 annealing can considerably reduce the V_O and thus lower the carrier density in In_2O_3 films [12-13]. The decrease in carrier density corresponds to the shift of the Fermi energy level (E_F) of In_2O_3 from deeply inside the conduction band into the bandgap, as depicted in **Fig. 3 (b)**. To verify the above E_F shifting model, first-principles simulation was adopted. The barrier energy and band structure calculations were performed using the Vienna Ab-initio Simulation Package (VASP) with Generalized Gradient Approximation (GGA) Perdew-Burke-Ernzerhof (PBE) exchange-correlation functionals being applied. The reciprocal k-point sampling was conducted with a resolution of 0.03 $Å^{-1}$ and an energy cutoff of 400 eV. The force tolerance was set to 0.05 eV/Å, and electronic convergence was set at 10^{-5} eV. The simulation results in **Fig. 3 (c)** substantiate the movement of E_F from above E_C to inside the bandgap of In_2O_3 when V_O decreases. The increase sheet resistance (R_{sh}) in **Fig. 3 (d)** also confirms the reduced carrier density after O_2 annealing. To sum up, by lowering the E_F and carrier density using O_2 annealing, E-mode In_2O_3 devices can be achieved [12-13].

However, the trade-off between annealing temperature and device performance should be emphasized. As the annealing

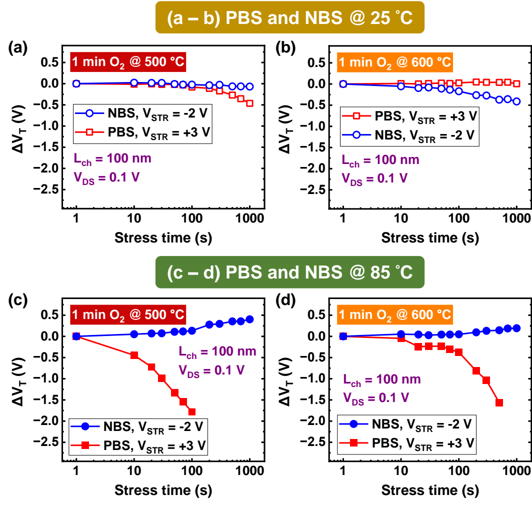

Fig. 4. Time evolution of ΔV_T of **(a)** 500 °C and **(b)** 600 °C devices after PBS and NBS tests at 25 °C. Time evolution of ΔV_T of **(c)** 500 °C and **(d)** 600 °C devices after PBS and NBS tests at 85 °C.

Ref	material	Structure	Thermal budget (°C)	L_{ch} (nm)	On/Off ratio	E-mode	V_T (V)	I_{ON} @ V_{DS} = 1 V (μA/μm)
5	IWO	DG	250	100	10^9	Yes	0.39	422
17	ITO	TG	300	50	7×10^9	No	-1.05	1680
6	IGZO	DG	300	30	4×10^8	Yes	0.29	690
3	**IGZO**	**TG**	**550**	**100**	**NA**	**No**	**-1**	**NA**
7	IGZO	TG	NA	40	$\sim10^8$	Yes	0.3	30
8	IGZO	VCT	NA	NA	$\sim10^8$	Yes	0.19	47
10	In_2O_3	TG	300	200	$> 10^9$	No	-0.48	193
11	In_2O_3	TG	300	100	5.2×10^4	No	< -5	2763
This Work	**In_2O_3**	**TG**	**600**	**100**	**4.3×10^9**	**Yes**	**1.00**	**216**

NA: not applied; DG: double-gate; TG: top-gate; VCT: vertical channel transistor

Table. I. Benchmarking of the reported top-gate oxide semiconductor transistors.

temperature increases from 500 to 600 °C, the reduction of carrier density results in a small decrease in drain current from 407 to 350 μA/μm at V_{DS} of 2 V (**Fig. 2 (b)** and **(c)**), a larger contact resistance (**Fig. 3 (d)**), and a smaller field-effect mobility (**Fig. 3 (e)**). If the process temperature further raises to 700 °C, a remarkable degradation of drain current around two orders, mobility down to < 1 cm²/V·s (**Fig. 3 (e)**), subthreshold swing ~ 282 mV/dec (**Fig. 3 (e)**) are observed. It is suspected that the 700 °C O_2 process not only reduces the carrier density but also degrades channel quality and interface quality.

Besides device performance, the reliability of high thermal budget In_2O_3 FETs was also examined and presented in **Fig. 4.** During positive bias stress (PBS)/negative bias stress (NBS) reliability tests, +3 V/-2 V was applied to the gate (gate stress voltage, V_{STR} = +3 V/-2 V) while the source and drain remained grounded. **Fig. 4 (a)** and **(b)** illustrate the extracted V_T change (ΔV_T) during PBS and NBS measurements at 25 °C from 500 °C and 600 °C transistors, respectively. Interestingly, 500 °C and 600 °C devices demonstrate two completely different ΔV_T trends during PBS and NBS tests at room temperature. The 500 °C/600 °C device shows a negative/negligible ΔV_T during PBS and a negligible/negative ΔV_T during NBS. The above V_T shift phenomenon can be explained by the competition of four major mechanisms (as shown in **Fig. 5**) [14-16]: 1) electron trapping with $\Delta V_T > 0$ [during PBS]; 2) electron de-trapping with $\Delta V_T < 0$ [during NBS]; 3) donor-like trap generation with $\Delta V_T < 0$ [during PBS]; 4) acceptor-like trap generation with $\Delta V_T > 0$ [during NBS]. During PBS operation, the effects of 1) electron trapping with $\Delta V_T > 0$ and 3) donor-like trap generation with $\Delta V_T < 0$ will compete and both contribute to the final V_T change. As for NBS, it becomes 2) electron de-trapping with $\Delta V_T < 0$ and 4) acceptor-like trap generation with $\Delta V_T > 0$ these two mechanisms against.

It is speculated that the donor-like and acceptor-like interface trap generations are suppressed in 600 °C In_2O_3 devices because of higher temperature annealing, which makes 1) electron trapping during PBS with $\Delta V_T > 0$ and 2) electron de-trapping during NBS with $\Delta V_T < 0$ the dominant mechanisms in reliability measurements, as demonstrated in **Fig. 5 (a)**. This leads to 600 °C In_2O_3 FETs with $\Delta V_T > 0$, which is negligible because mechanisms 1) and 3) compensate, during PBS and $\Delta V_T < 0$ during NBS (**Fig. 4 (b)**). On the other hand, in 500 °C In_2O_3 devices, 3) donor-like with $\Delta V_T < 0$ and 4) acceptor-like with $\Delta V_T > 0$ trap generations are more important and result in the different ΔV_T shift trend (**Fig. 4 (a)**) compared with 600 °C transistors, as presented in **Fig. 5 (b)**. However, this does not mean electron trappings/de-trappings do not play any role in 500 °C In_2O_3 FETs. One can notice the 500 °C In_2O_3 FET in **Fig. 4 (b)** exhibits an $\Delta V_T < 0$ during NBS, which implies the presence of electron de-trapping at the dielectric/In_2O_3 interface. **Fig. 4 (c-d)** shows the PBS and NBS tests at higher temperature of 85 °C. Under elevated temperatures, more chemical bonds are easy to break and more interface traps are generated, leading to larger ΔV_T. **Table I** benchmarks our 100 nm short-channel length top-gate In_2O_3 FETs with other reported top-gate oxide semiconductor transistors including [3], which also investigated high thermal budget devices but with negative V_T at around -1V. This work is the first top-gate E-mode oxide-semiconductor transistors that demonstrate high thermal budget (>550 °C) compatibility for DRAM processes.

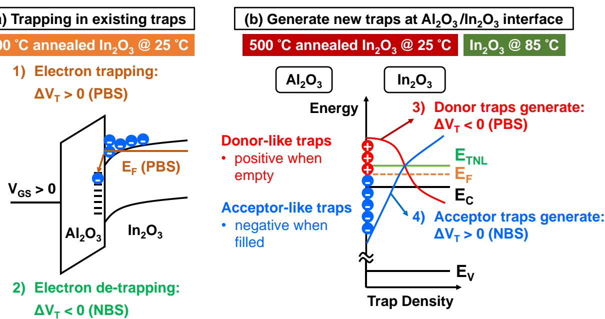

Fig. 5. Possible mechanisms of V_T shifts during PBS and NBS reliability test. (a) V_T shifts result from charge trapping and de-trapping in existing traps. These are the more dominant mechanisms for 600 °C annealing devices. (b) V_T shifts caused by donor-like and acceptor-like interface trap generations. These are the more dominant mechanisms for 500 °C annealing devices and for devices at environmental temperature of 85 °C.

IV. Conclusion

In conclusion, we report the first top-gate E-mode In_2O_3 FETs with 600 °C O_2 annealing that satisfies the high thermal budget requirement (> 550 °C) for DRAM process. With E-mode, high thermal budget, ultralow off-current (~10^{-14} A/μm), and good on-current (I_{ON}) of 216 μA/μm (at V_{DS} = 1 V), In_2O_3 FETs have the potential for future oxide-semiconductor DRAM applications.

References

[1] A. Belmonte *et al.*, "Lowest $I_{OFF} < 3\times10^{-21}$ A/µm in capacitorless DRAM achieved by Reactive Ion Etch of IGZO-TFT," *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan, 2023, pp. 1-2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185398.

[2] A. Belmonte *et al.*, "Tailoring IGZO-TFT architecture for capacitorless DRAM, demonstrating > 10^3s retention, >10^{11} cycles endurance and Lg scalability down to 14 nm," *2021 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2021, pp. 10.6.1-10.6.4, doi: 10.1109/IEDM19574.2021.9720596.

[3] W. Kim et al., "Demonstration of crystalline IGZO transistor with high thermal stability for memory applications," 2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Kyoto, Japan, 2023, pp. 1-2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185258.

[4] R. Ritzenthaler et al., "A new high-k/metal gate CMOS integration scheme (Diffusion and Gate Replacement) suppressing gate height asymmetry and compatible with high-thermal budget memory technologies," 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 2014, pp. 32.3.1-32.3.4, doi: 10.1109/IEDM.2014.7047154.

[5] H. Ye *et al.*, "Double-Gate W-Doped Amorphous Indium Oxide Transistors for Monolithic 3D Capacitorless Gain Cell eDRAM," *2020 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2020, pp. 28.3.1-28.3.4, doi: 10.1109/IEDM13553.2020.9371981.

[6] K. Chen *et al.*, "Scaling Dual-Gate Ultra-thin a-IGZO FET to 30 nm Channel Length with Record-high $G_{m,max}$ of 559 µS/µm at V_{DS}=1 V, Record-low DIBL of 10 mV/V and Nearly Ideal SS of 63 mV/dec," *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2022, pp. 298-299, doi: 10.1109/VLSITechnologyandCir46769.2022.9830389.

[7] S. Subhechha *et al.*, "Ultra-low Leakage IGZO-TFTs with Raised Source/Drain for $V_t > 0$ V and $I_{on} > 30$ µA/µm," *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2022, pp. 292-293, doi: 10.1109/VLSITechnologyandCir46769.2022.9830448.

[8] D. Ha *et al.*, "Highly Manufacturable, Cost-Effective, and Monolithically Stackable $4F^2$ Single-Gated IGZO Vertical Channel Transistor (VCT) for sub-10nm DRAM," *2023 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2023, pp. 1-4, doi: 10.1109/IEDM45741.2023.10413772.

[9] S. Wahid *et al.*, "Effect of Top-Gate Dielectric Deposition on the Performance of Indium Tin Oxide Transistors," in *IEEE Electron Device Letters*, vol. 44, no. 6, pp. 951-954, June 2023, doi: 10.1109/LED.2023.3265316.

[10] M. Si, Z. Lin, Z. Chen and P. D. Ye, "High-Performance Atomic-Layer-Deposited Indium Oxide 3-D Transistors and Integrated Circuits for Monolithic 3-D Integration," in *IEEE Transactions on Electron Devices*, vol. 68, no. 12, pp. 6605-6609, Dec. 2021, doi: 10.1109/TED.2021.3106282.

[11] P. -Y. Liao *et al.*, "Transient Thermal and Electrical Co-Optimization of BEOL Top-Gated ALD In_2O_3 FETs on Various Thermally Conductive Substrates Including Diamond," *2022 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2022, pp. 12.4.1-12.4.4, doi: 10.1109/IEDM45625.2022.10019438.

[12] M. Si, A. Charnas, Z. Lin and P. D. Ye, "Enhancement-Mode Atomic-Layer-Deposited In_2O_3 Transistors With Maximum Drain Current of 2.2 A/mm at Drain Voltage of 0.7 V by Low-Temperature Annealing and Stability in Hydrogen Environment," in *IEEE Transactions on Electron Devices*, vol. 68, no. 3, pp. 1075-1080, March 2021, doi: 10.1109/TED.2021.3053229.

[13] J. Zhang *et al.*, "First Demonstration of BEOL-Compatible Atomic-Layer-Deposited InGaZnO TFTs with 1.5 nm Channel Thickness and 60 nm Channel Length Achieving ON/OFF Ratio Exceeding 1011, SS of 68 mV/dec, Normal-off Operation and High Positive Gate Bias Stability," *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Kyoto, Japan, 2023, pp. 1-2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185312.

[14] Y. -P. Chen, M. Si, B. K. Mahajan, Z. Lin, P. D. Ye and M. A. Alam, "Positive Bias Temperature Instability and Hot Carrier Degradation of Back-End-of-Line, nm-Thick, In_2O_3 Thin-Film Transistors," in *IEEE Electron Device Letters*, vol. 43, no. 2, pp. 232-235, Feb. 2022, doi: 10.1109/LED.2021.3134902.

[15] A. Charnas, M. Si, Z. Lin and P. D. Ye, "Improved Stability With Atomic-Layer-Deposited Encapsulation on Atomic-Layer In_2O_3 Transistors by Reliability Characterization," in *IEEE Transactions on Electron Devices*, vol. 69, no. 10, pp. 5549-5555, Oct. 2022, doi: 10.1109/TED.2022.3198926.

[16] Z. Zhang *et al.*, "Reliability of Atomic-Layer-Deposited Gate-All-Around In_2O_3 Nano-Ribbon Transistors with Ultra-High Drain Currents," *2022 International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2022, pp. 30.3.1-30.3.4, doi: 10.1109/IEDM45625.2022.10019494.

[17] C. Gu *et al.*, "High-Performance Short-Channel Top-Gate Indium-Tin-Oxide Transistors by Optimized Gate Dielectric," in *IEEE Electron Device Letters*, vol. 44, no. 5, pp. 837-840, May 2023, doi: 10.1109/LED.2023.3262684.