Exam 1

ECE 559: MOS VLSI Design (Fall 2009)

ECE Department, Purdue University

October 1, 2009

Name: SOLUTION

PUID: _____

Instructions: It is important that you clearly show your work and mark the final answer clearly, closed book, closed notes, no calculator.

Time: 1 hour 15 minutes

Scoring

Problem 1 (Total 30 points)

Part a) 15 points _____

Part b) 15 points _____

Problem 2 (Total 30 points)

Part a) 15 points _____

Part b) 15 points _____

Problem 3 (Total 40 points)

Part a) 30 points _____

Part b) 10 points _____

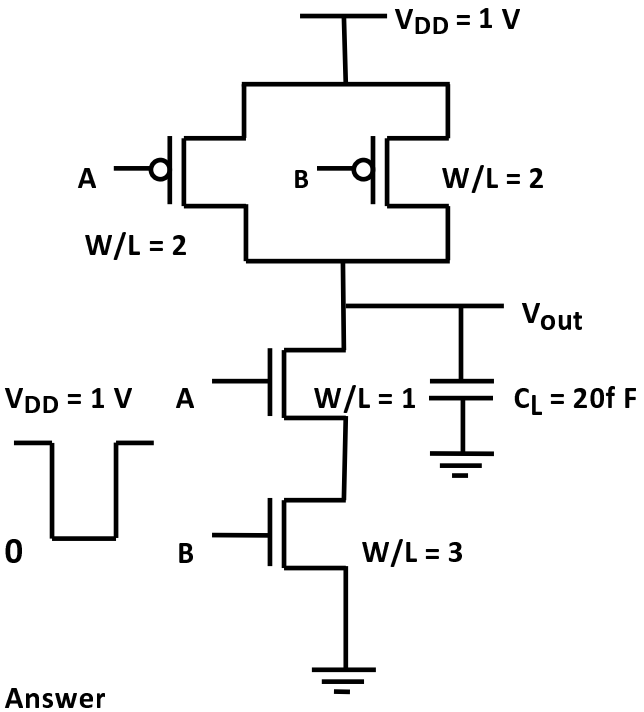
Total: 100 points _____

Problem 1: For the circuits and conditions given below, determine the energy dissipated. Clearly specify your assumptions, if any.

[30 points]

Part a) Inputs A and B are switching simultaneously from **V_{DD} to 0 followed by 0 to V_{DD}**. Assume V_{out} = 0 initially.

[15 points]



$K_p' = \mu_p C_{ox}$ = 30e-6 A/V^2

$K_n' = \mu_n C_{ox}$ = 60e-6 A/V^2

V_{tp} = -0.3 V, V_{tn} = 0.3 V

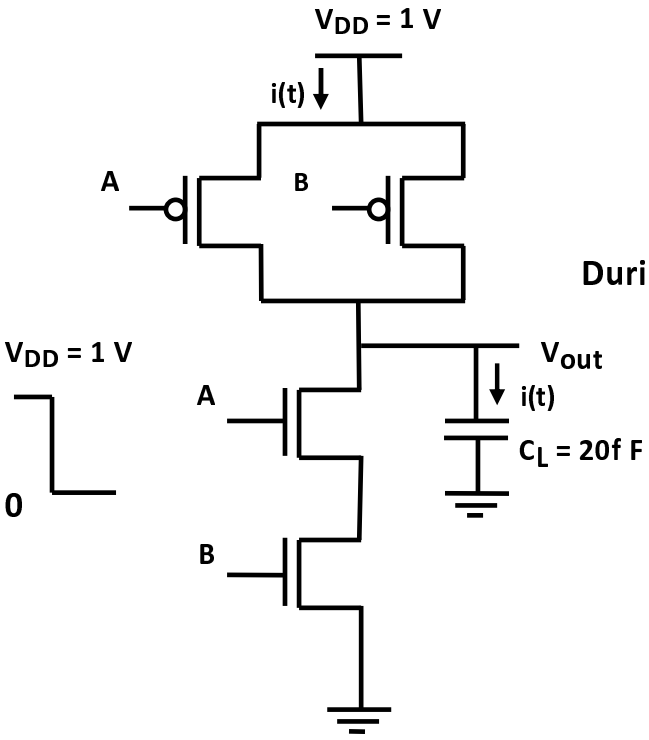
Answer

When the inputs A and B simultaneously switch from V_{DD} to 0, the PMOS network gets ON and current is drawn from supply that charges the output node capacitance C_L to V_{DD}. Energy drawn from supply

$$E_{V_{DD}} = \int i(t) V_{DD} dt = \int_0^{V_{DD}} C_L V_{DD} dV_{out} = C_L V_{DD}^2.$$

Energy stored in the capacitor C_L,

$$E_{stored,C_L} = \int i(t) V_{out} dt = \int_0^{V_{DD}} C_L V_{out} dV_{out} = \frac{1}{2} C_L V_{DD}^2.$$

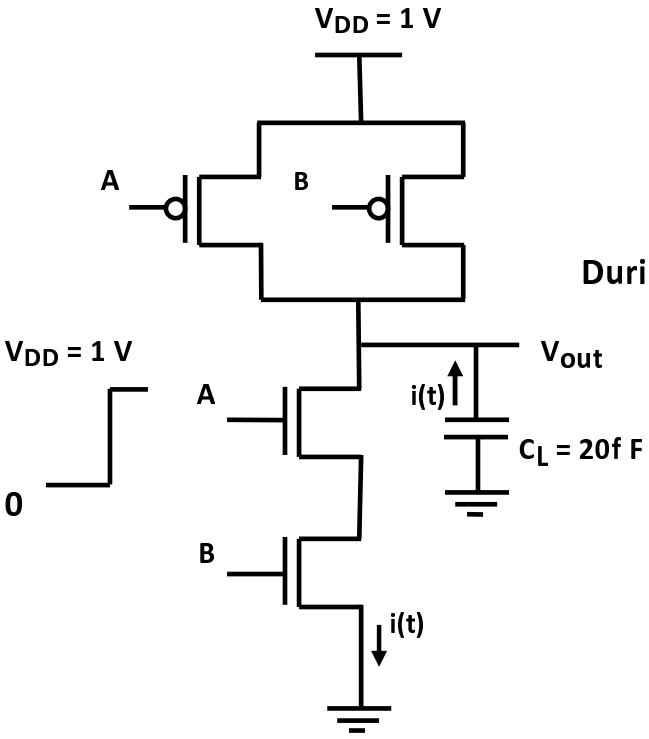


During Charging

$$i(t) = C_L \frac{dV_{out}}{dt}.$$

So,

$$E_{dissipated,0\to1} = E_{V_{DD}} - E_{stored,C_L} = \frac{1}{2} C_L V_{DD}^2.$$



During discharging

$$i(t) = -C_L \frac{dV_{out}}{dt}.$$

When the inputs A and B simultaneously switch from *0 to V_{DD}*, the NMOS network gets ON and the output node capacitance C_L gets discharged to *0.*

$$E_{dissipated,1\to 0} = \int i(t)V_{out}dt = \int_{V_{DD}}^{0} -C_L V_{out} dV_{out} = \frac{1}{2}C_L V_{DD}^2$$

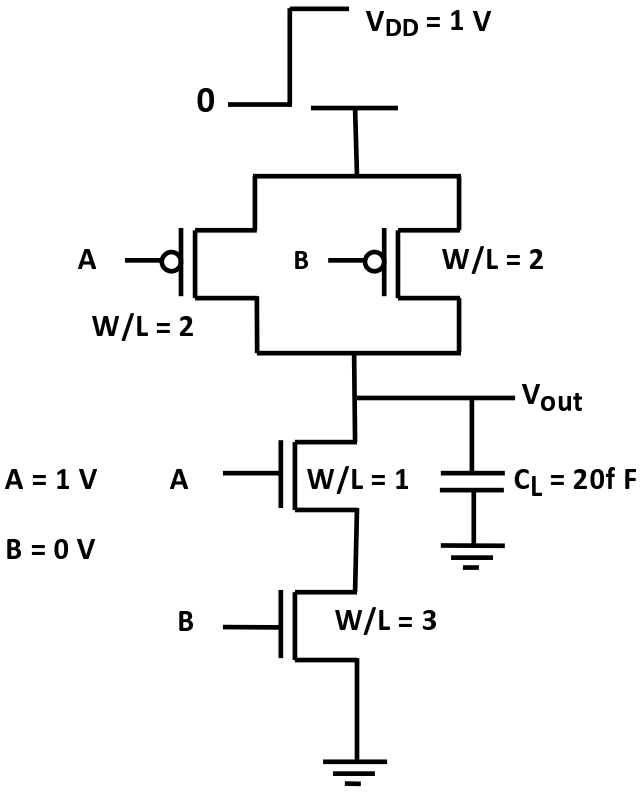
So total energy dissipated

$$E_{total} = E_{dissipated,1\to 0} + E_{dissipated,0\to 1} = \frac{1}{2}C_L V_{DD}^2 + \frac{1}{2}C_L V_{DD}^2 = C_L V_{DD}^2$$

Putting C_L = 20f F and V_{DD} = 1 V,

$E_{dissipated,total}$ = 20 f Joule

Part b) The voltage at the supply terminal is switching from **0 to V_{DD}**. Assume A = 1 V and B = 0. **[15 points]**



$K_p' = \mu_p C_{ox}$ = 30e-6 A/V^2

$K_n' = \mu_n C_{ox}$ = 60e-6 A/V^2

V_{tp} = -0.3 V, V_{tn} = 0.3 V

When the inputs A = 1 V and B = 0, the PMOS network gets ON and current is drawn from supply that charges the output node capacitance C_L to V_{DD}. Energy drawn from source

$$E_{V_{DD}} = \int i(t) V_{DD} dt = \int_0^{V_{DD}} C_L V_{DD} dV_{out} = C_L V_{DD}^2.$$

Energy stored in the capacitor C_L,

$$E_{stored,C_L} = \int i(t) V_{out} dt = \int_0^{V_{DD}} C_L V_{out} dV_{out} = \frac{1}{2} C_L V_{DD}^2.$$

So,

$$E_{dissipated,0\to1} = E_{V_{DD}} - E_{stored,C_L} = \frac{1}{2} C_L V_{DD}^2.$$

Putting C_L = 20f F and V_{DD} = 1 V,

$E_{dissipated}$ = 10 f Joule

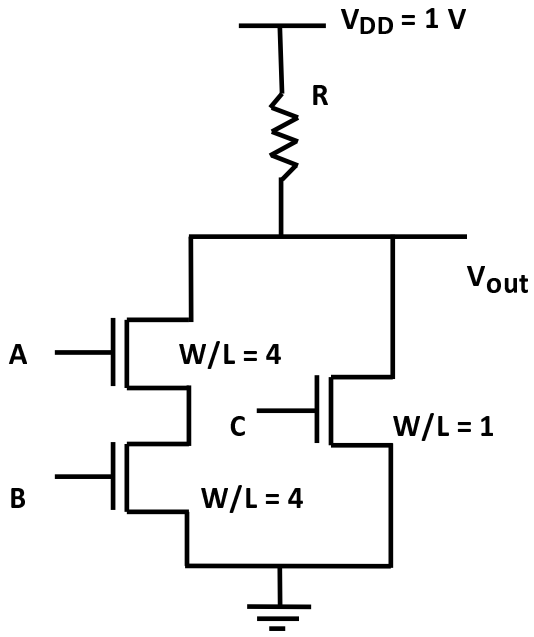
Problem 2:

[30 points]

Part a) For the circuit shown below, find the **minimum value of R** so that V_{OL} = 0.2 V. V_{OL} represents the output low voltage. Clearly state all of your assumptions.

What will be the V_{OH}? V_{OH} represents the output high voltage. Explain your answer.

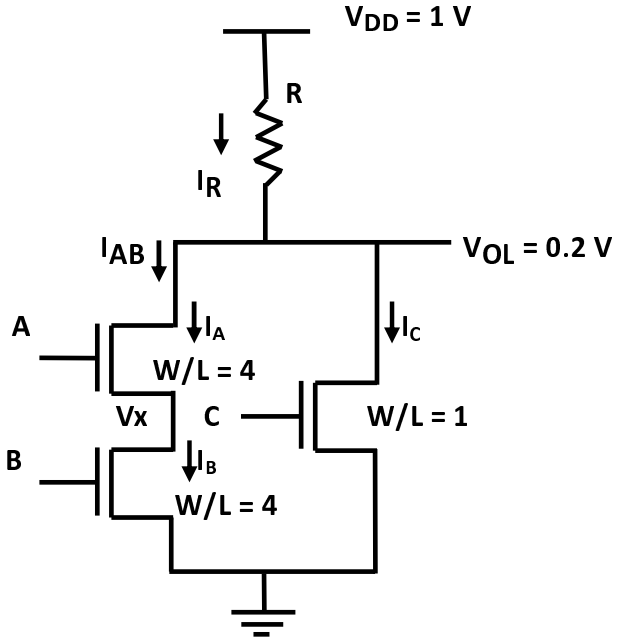
[15 points]



$K_n' = \mu_n C_{ox}$ = 40e-6 A/V^2

V_{tn} = 0.3 V

Answer



$K_n' = \mu_n C_{ox}$ = 40e-6 A/V^2

V_{tn} = 0.3 V

$$I_R = \frac{V_{DD} - V_{OL}}{R} = \frac{1 - 0.2}{R} = \frac{0.8}{R}.$$

I_R has to be equal to the current flowing through the NMOS network as they are serially connected, i.e.

$$I_R = I_{NMOS} = I_{AB} + I_C.$$

To get the **minimum value of R**, I_R has to be maximum, i.e., I_{NMOS} has to be maximum. The output low voltage is achieved when A = B = 1 or C = 1 and of course when A = B = C = 1. Accordingly, if all the NMOS transistors are ON, i.e., A = B = C = 1 (as OFF current is assumed to be zero), the minimum value of R is achieved.

To calculate I_{AB} we have to determine the voltage at the intermediate node, V_X. Both the NMOSs with inputs A and B will be apparently in *linear* region. This is because of the reason that there is only 0.2 V to be dropped across both the transistors and for both of them the linear region condition would be satisfied, i.e.,

$V_{ds,A} < V_{GS,A} - V_{tn}$ and $V_{ds,B} < V_{GS,B} - V_{tn}$.

Anyway, we can double-check later on after finding the voltage V_X. Since the NMOSs with inputs A and B are serially connected

$$I_{AB} = I_A = I_B$$

$$\Rightarrow \left((1.0 - 0.3 - vx) * (0.2 - vx) - \frac{(0.2 - vx)^2}{2} \right) = \left((1.0 - 0.3) * vx - \frac{vx^2}{2} \right)$$

$$\Rightarrow \left((0.7 - vx) * (0.2 - vx) - \frac{(0.2 - vx)^2}{2} \right) = \left(0.7 * vx - \frac{vx^2}{2} \right).$$

Since, V_X has to be less than 0.2 V and the transistor with input A is ON, we can neglect V_X with respect to 0.7 V. Also, body effect is not considered here. Accordingly,

$$\left(0.7 * (0.2 - vx) - \frac{(0.2 - vx)^2}{2} \right) = \left(0.7 * vx - \frac{vx^2}{2} \right)$$

$$\Rightarrow 0.2 - vx = vx$$

$$\Rightarrow vx = 0.1$$

We can verify now that both of the NMOSs are indeed in linear region.

$$I_R = I_{NMOS} = I_{AB} + I_C = I_B + I_C$$

$$\Rightarrow \frac{0.8}{R} = 40*10^{-6}\left(4*\left(0.7*0.1-\frac{0.1^2}{2}\right)+1*\left(0.7*0.2-\frac{0.2^2}{2}\right)\right)$$

$$\Rightarrow \frac{0.8}{R} = 40*10^{-6}\left(4*0.065+1*0.12\right)$$

$$\Rightarrow \frac{0.8}{R} = 40*10^{-6}*0.38$$

$$\Rightarrow \frac{0.8}{R} \simeq 40*10^{-6}*0.40$$

$$\Rightarrow R \simeq 5*10^4\,\Omega$$

So,

$R_{minimum}$ = 50 KΩ

In the previous calculation we have assumed different V_{OL} for different input vector combinations and calculated the minimum R. If V_{OL} is assumed to be the *output low voltage for all the possible input combinations*, then we have to consider only the highest-resistance path from output to ground when the output is low because that will cause the *highest* V_{OL} at the output. We need choose the *minimum* R for which the *highest* V_{OL} will occur because if R is more than a minimum value, V_{OL} will just go lower. Accordingly, we need to consider only I_C because that corresponds to the lowest ON current through the NMOS network when the NMOS network is ON and the output is low. So,

$$\frac{0.8}{R} = 40*10^{-6}*1*\left(0.7*0.2-\frac{0.2^2}{2}\right)$$

$$\Rightarrow \frac{0.8}{R} = 40*10^{-6}*1*0.12$$

$$\Rightarrow R = 16.7*10^4\,\Omega.$$

Accordingly,

$R_{minimum}$ = 167 KΩ

Note: Full credit will be given to any of the two approaches.

When NMOS network is off (for certain combinations of the inputs A, B, and C), the current flowing through the resistor R will eventually charge the output node capacitance. The charging time will vary depending on the value of R but eventually the output is going to charge up to V_{DD}. So,

$$\boxed{V_{OH} = 1\ V}$$

Part b) For the part a), explain qualitatively the **result of body effect** on V_{OL} and V_{OH}.

[15 points]

Result of body effect on V_{OL}

Since the substrate and source nodes for the NMOS with input A are not at the same potential, the NMOS will experience an increase in threshold voltage. So eventually the total current flowing through the NMOS network, I_{NMOS} would decrease. But,

$$I_R = I_{NMOS}.$$

So

$$V_{out} = V_{DD} - I_R R$$

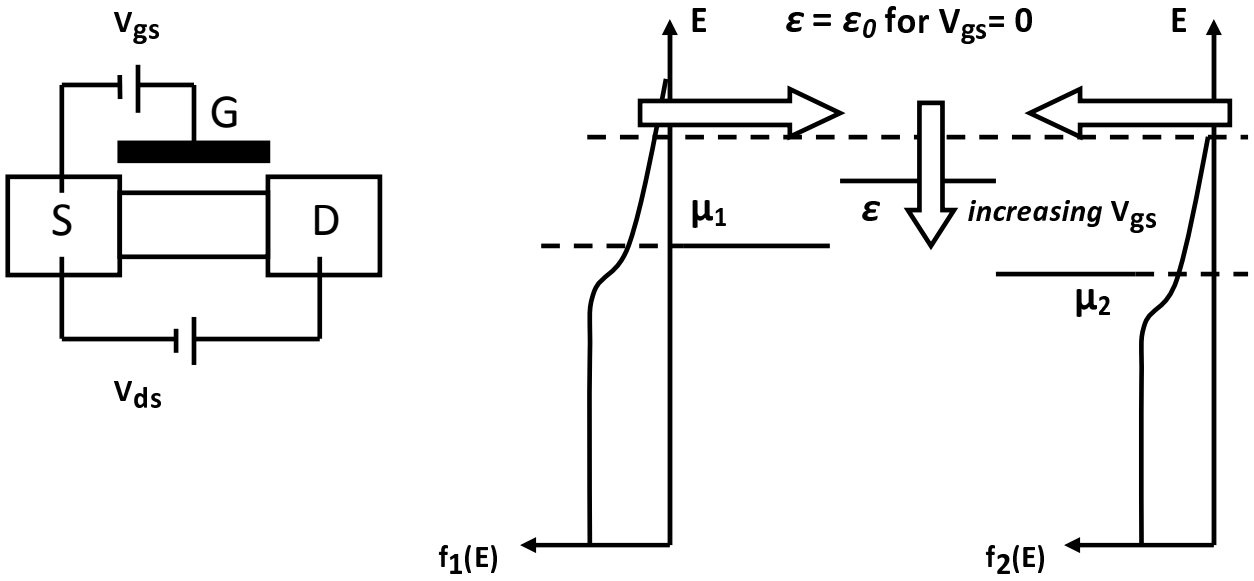
would increase. Hence, **V_{OL} will increase**.

Result of body effect on V_{OH}

Since during the determination of V_{OH} we consider the NMOS network to be off and we have only a resistor connecting V_{DD} to V_{out}, **body effect will not affect V_{OH}**.

Problem 3:

[40 points]



Part a) For the NMOS shown above, derive an **expression of electron current** flowing from source (S) to Drain (D). μ_1, μ_2 are electro-chemical potential energies at the source and drain terminals, respectively. The Fermi distribution function *f(E)* specifies, under equilibrium conditions, the probability that an available state at an energy E will be occupied by an electron.

$$f(E) = \frac{1}{1 + e^{\frac{(E - E_F)}{KT}}}$$

where E_F is the Fermi level. Clearly show your steps, specify your assumptions, and name the parameters you are using.

[30 points]

Answer

The electron current that is flowing from source to drain (I_{SD}) and drain to source (I_{DS}) can be written as

$$I_{sd} = qAn_+v_+$$
$$I_{ds} = qAn\_v\_$$

where

q = single electron charge (C),
A = cross-sectional area (cm^2) of source/drain,
n_+= number of electrons/cm^3 traversing from source to drain,
n_-= number of electrons/cm^3 traversing from drain to source,
v_+= average velocity (cm/sec) of the electrons traversing from source to drain,
v_-= average velocity (cm/sec) of the electrons traversing from drain to source.

Note that, the unit of I_{sd} and I_{ds} are in *Ampere*.

In general we can assume,

$$v_+ = v_- = v.$$

We know that the number of electrons,

n = density of states*Fermi function.

Since, we have only one energy level, we will have density of states as 1. Accordingly,

$$n_+ = f_1(\varepsilon) = \frac{1}{1+e^{\frac{(\varepsilon-\mu_1)}{KT}}} \simeq e^{-\frac{(\varepsilon-\mu_1)}{KT}} \qquad \text{for } (\varepsilon - \mu_1) >> KT$$

$$n_- = f_2(\varepsilon) = \frac{1}{1+e^{\frac{(\varepsilon-\mu_2)}{KT}}} \simeq e^{-\frac{(\varepsilon-\mu_2)}{KT}} \qquad \text{for } (\varepsilon - \mu_2) >> KT$$

Since, according to the figure provided, we have put some positive voltage at node D with respect to source node S,

$$\mu_1 > \mu_2$$
$$\Rightarrow n_+ > n_-$$

Accordingly, there will be a net electron current flowing from source to drain, i.e.,

$$I = I_{sd} - I_{ds} = qAv(n_+ - n_-)$$

$$\Rightarrow I = qAv\left(e^{-\frac{(\varepsilon-\mu_1)}{KT}} - e^{-\frac{(\varepsilon-\mu_2)}{KT}} \right)$$

$$\Rightarrow I = qAve^{-\frac{(\varepsilon-\mu_1)}{KT}}\left(1 - e^{-\frac{(\mu_1-\mu_2)}{KT}} \right)$$

$$\Rightarrow I = qAve^{-\frac{(\varepsilon-\mu_1)}{KT}}\left(1 - e^{-\frac{(\mu_1-\mu_2)}{KT}} \right)$$

$$\Rightarrow I = qAve^{-\frac{(\varepsilon_0-\mu_1)}{KT}} e^{\frac{(\varepsilon_0-\varepsilon)}{KT}}\left(1 - e^{-\frac{(\mu_1-\mu_2)}{KT}} \right)$$

Now, we can write

$$\mu_1 - \mu_2 = qV_{DS}$$

$$\varepsilon_0 - \varepsilon = \frac{qV_{GS}}{m}$$

where, *m* is the body-bias coefficient. It arises from the fact that when a voltage V_{GS} (gate-to-source voltage) is applied, there is some voltage drop that happens across the gate oxide as well. Thus only a part of the voltage applied is responsible to shifting the gate energy level downward. Thus, m > 1 in general. So,

$$I = qAve^{-\frac{(\varepsilon_0-\mu_1)}{KT}} e^{\frac{V_{GS}}{mKT}}\left(1 - e^{-\frac{qV_{DS}}{KT}} \right)$$

$$\Rightarrow I = I_0 e^{\frac{V_{GS}}{mKT}}\left(1 - e^{-\frac{qV_{DS}}{KT}} \right)$$

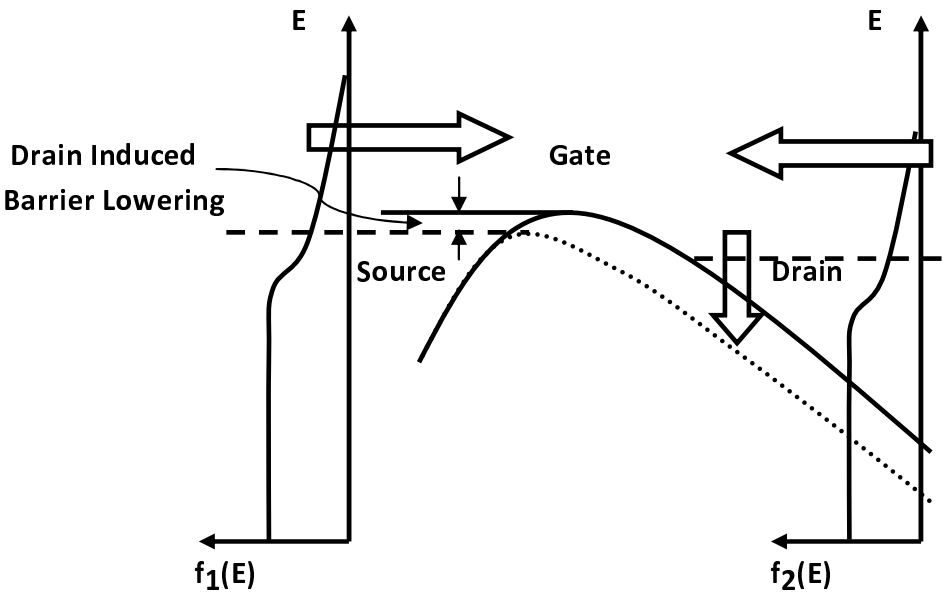
where,

$$I_0 = qAve^{-\frac{(\varepsilon_0-\mu_1)}{KT}}.$$

Part b) Explain qualitatively the **effect of Drain Induced Barrier Lowering (DIBL)** on the current that you have derived in part a).

[10 points]

When a positive voltage at drain is applied (with respect to source), it lowers the effective barrier height as shown in the below figure. Ideally gate only should have control over determining the barrier height. But, drain gets also some control as it is electrostatically coupled to the gate.



So due to DIBL, the electrons going from source-to-drain and drain-to-source both are (exponentially) increased. But as the Fermi level at drain is at lower potential than that of the source, the increase in the number of electrons traversing from source-to-drain is more than that of for drain-to-source. Accordingly, **the current that is calculated in part a) would get increased**.