



2002 DIGEST OF TECHNICAL PAPERS AND VISUALS SUPPLEMENT

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Welcome

2002
International
Solid-State
Circuits
Conference

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Thank you and Enjoy!
Laura Chizuko Fujino
ISSCC Director of Publications/Presentations
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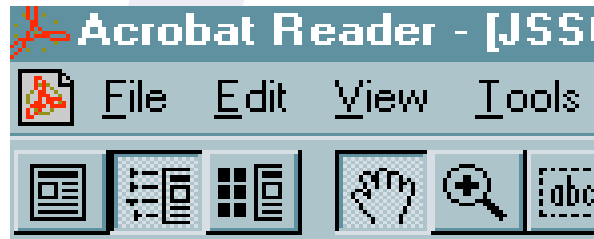
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NAVIGATION BUTTONS

This Guide contains a variety of navigational aids to help you easily explore the contents.

Section Map

The Electronic Guide is constructed in sections: e.g. Papers, Authors, Getting Started. The current section is shown at the top of each page. The “path” to this section is shown at the right. Clicking these text buttons moves you to the start of that section.

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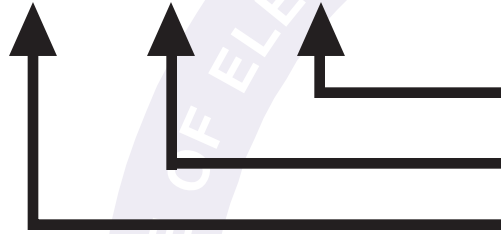
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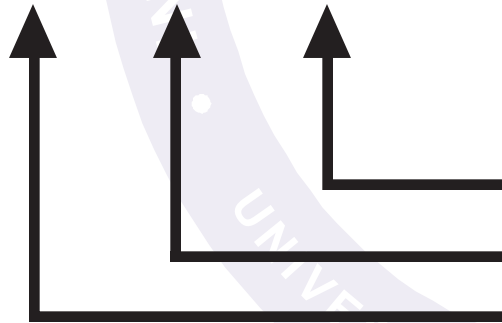
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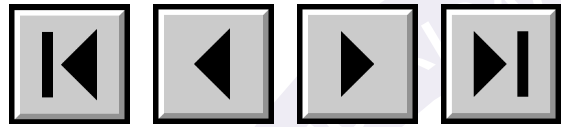
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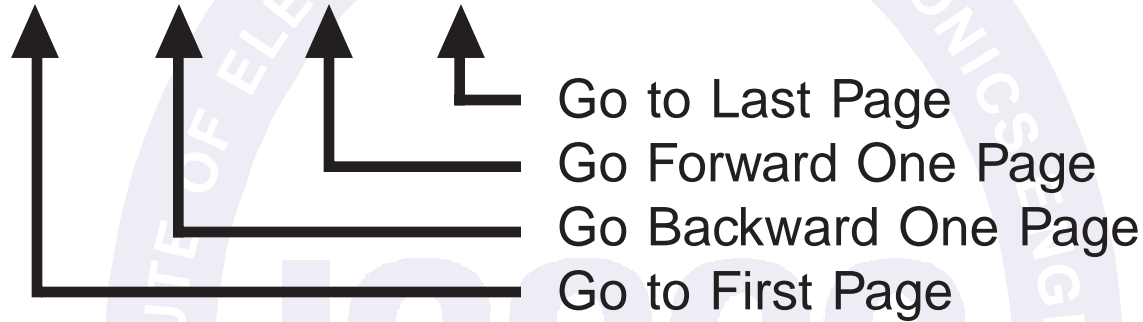


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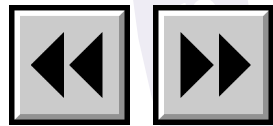
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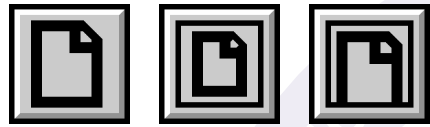


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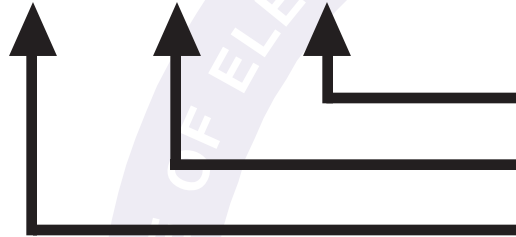


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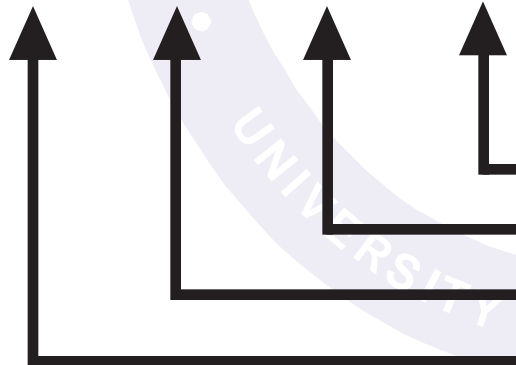
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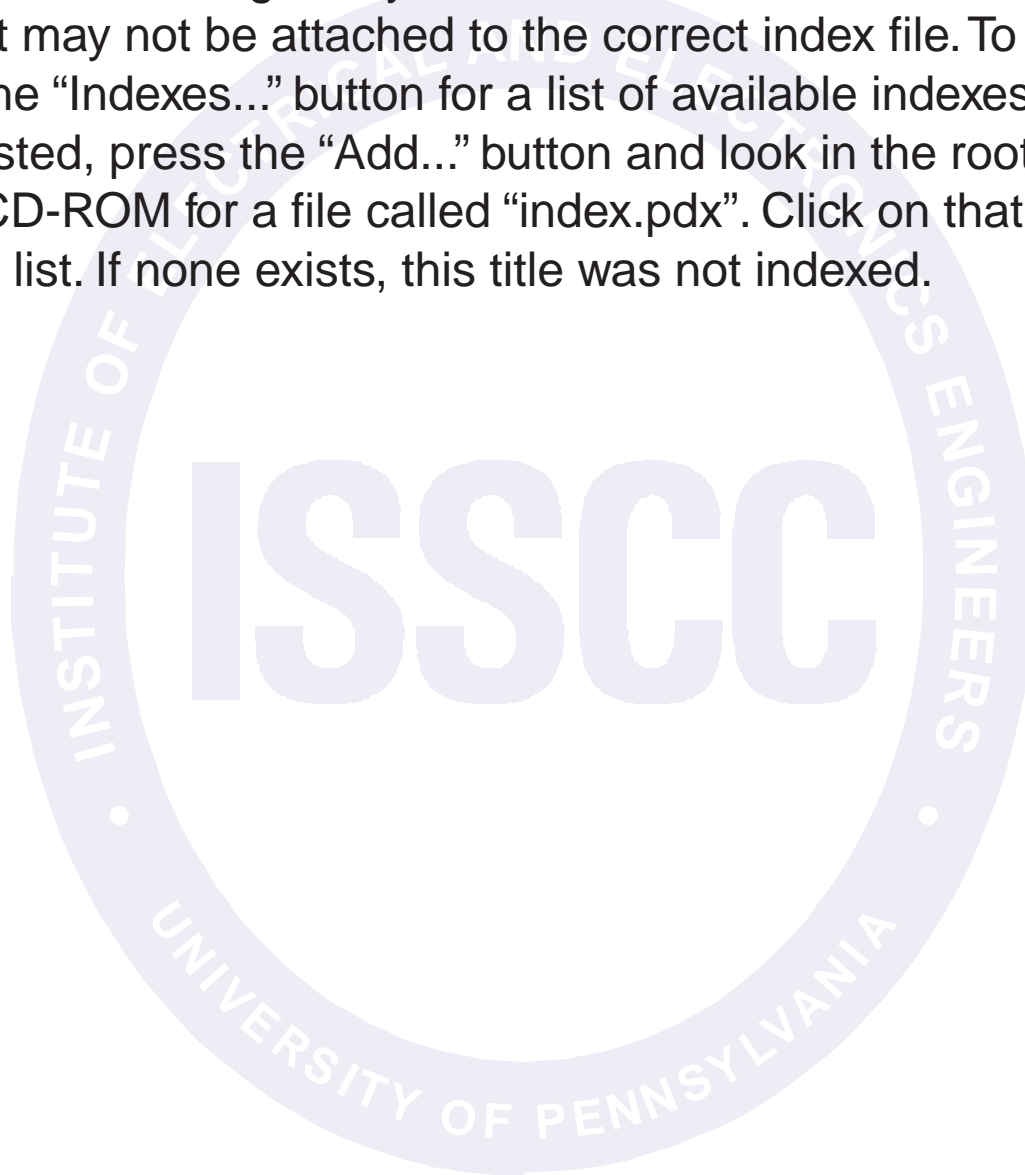
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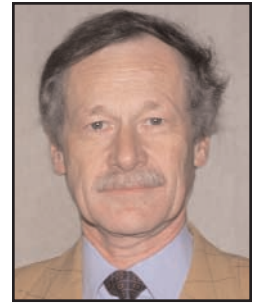
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Foreword

ICs for Information Technologies



Welcome to the 49th annual ISSCC. ISSCC 2002 promises to be exciting and continues the proud tradition of ISSCC as the foremost global forum for presentation of advances in solid-state circuits. ISSCC 2002 consists of a record 171 technical papers in 25 Sessions, a three-paper Plenary Session, two special-topic evening sessions, eight evening panels, seven tutorials, two short courses and one workshop. The geographical distribution of the papers illustrates the truly international character of the Conference. This year, 50% of the accepted papers are from North America, 22% from Europe, and 28% from the Far East. As usual, 70% are from industry and 30% from universities.

Information Technologies find applications in all aspects of life. They allow higher efficiency in managing work load but they also narrow the gap with families and friends. This is why ICs in information technologies cover all technical aspects from memories to disposable sensors, from wireless and wireline communications to basic analog and digital circuits. A short overview makes this clear.

In wireless communications, 0.18 μ m CMOS has become the mainstream technology, leading to a Bluetooth radio in Session 5 and a direct conversion receiver for UMTS in Session 4. This is also true for the most advanced analog realizations such as a 4MHz 4b 5th-order sigma-delta converter with only 8x oversampling Session 13. The fastest analog chip, however, is the 4GSample/s 8b CMOS ADC which exploits parallelism by interleaving 32 pipeline ADCs in a standard 0.35 μ m CMOS technology (Session 10). The lowest voltage supply is a mere 0.7V (with threshold voltages of 0.43V and -0.38V) for a MOSFET-only 12b sigma-delta modulator, again in a 0.18 μ m CMOS technology.

Technologies are not yet standardized for ADSL drivers, however. Session 19 divulges realizations in complementary bipolar on SOI, on 0.35 μ m BICMOS and on 0.5 μ m CMOS. Other impressive wireline communications chips are a SONET OC-192 receiver and transmitter at 10Gb/s in 0.18 μ m CMOS (Session 15).

The highest frequency clocks are, as usual, provided by the processor chips. A 64b microprocessor runs at 1.1GHz in a 0.13 μ m CMOS technology with copper (Session 23). It contains 90M transistors and consumes 53W. Power savings can be realized, however, by active forward biasing the pMOSTs reducing the VTs by 0.2V so that the 0.13 μ m chip can run at 1.1V instead of 1.3V (Session 16). The highest frequency clock is 6.5GHz for a single-ended dynamic ALU again in 0.13 μ m CMOS (Session 25).

In memories, a 1Gb NAND Flash memory is reported in 0.13 μ m CMOS (Session 6) but also a nonvolatile 32Mb ferroelectric RAM (Session 9). A 0.13 μ m InP HEMT technology is used for a 90Gb/s multiplexer (Session 11) but a conventional 0.18 μ m CMOS technology for a 44Gb/s switching processor (Session 3).

Finally, there are several sensor sessions highlighting a 3-M pixel CCD chip allowing 60 images per second (Session 2) and a single-chip gyroscope (Session 26), but also a CMOS sensor array for DNA detection (Session 21). And there is much more.

Many people have contributed to the success of ISSCC 2002. The US, Far East, European and Executive Committees are composed of 168 experts who met in April, June, August, September, and October to plan the conference. I express gratitude and appreciation to all of them. In particular, I thank Watanabe-san the Far-East Chair, Arai-san the Far-East Secretary, Yamashina-san the Far-East Assistant Secretary, Rudy Van de Plassche the European Chair, Jan Sevenhans the European Vice-Chair and Albert Theuwissen the European Secretary, for leadership, assistance and support. I thank the Subcommittee Chairs for tremendous efforts: Behzad Razavi (Analog), Ian Young (Digital), Dennis Polla (Imagers, Displays & MEMS), Bruce Bateman (Memory), Wanda Gass (Signal Processing), Bill Bowhill (Technology Directions), Trudy Stetzler (Wireless Communications), and Russ Apfel (Wireline Communications). Their leadership and the efforts of their subcommittees have resulted in a quality Conference again this year. I express appreciation to all members of the ISSCC Program Committee for the tremendous commitment of time and expertise. I thank all of the authors and speakers for their contributions to making this year's Conference more than worth attending.

Additionally, I express thanks; to Anantha Chandrakasan for valuable assistance as Vice-Chair; to Diane Suiters and her colleagues at Courtesy Associates for Conference arrangements, operations, registration, and valuable assistance; to the staff at MiraCD for helping the migration to electronic submission format; to John Wuorinen for his editorial skills; to Steve Bonney of J.S. McCarthy for help in producing the Advance Program and Digest; to Ken Smith and Laura Fujino for extensive work with the Press Kit, press conferences, awards, CDROM, and visuals supplement; to Frank Hewlett for keeping track of action items and Web operations; and to Dave Pricer for financial awareness. A special thank-you goes to Tim Tredwell for support, guidance, and leadership.

I know you will find this year's Conference revealing, rewarding, and enjoyable.

A handwritten signature in black ink, appearing to read 'W. Sansen'.

Willy Sansen, ISSCC 2002 Program Committee Chair

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Short Course

WIDEBAND COMMUNICATIONS

This Short Course is intended to jumpstart engineers in the design and development of CMOS circuits for wideband optical and gigabit Ethernet communication applications. Course completion provides an overall perspective of system tradeoffs along with detailed circuit design strategies for key circuit building blocks. Topics covered include an overview of transceiver architectures and key metrics of wideband amplifiers, chip-to-chip communication and clock and data recovery.

OUTLINE

HIGH-SPEED DSP-BASED TRANSCEIVERS



This first segment of the short course describes standard techniques used in high-speed DSP-based transceivers, such as modulation, equalization, Viterbi detection, and forward error correction, with special emphasis on architecture and VLSI implementation. It then studies two specific design cases: Gigabit Ethernet over unshielded twisted pair, and a DSP-based optical transceiver.

Instructor: Kamran Azadet received PhD from ENST Paris in 1994. Since 1994 he has been with Bell Labs/Holmdel NJ, working on color digital CMOS cameras, and high-speed transceivers. He was a member of the IEEE 802.3ab Gigabit Ethernet 1000BaseT and 10 Gigabit Ethernet 802.3ae standard committees. He is currently director of the high-speed Communications VLSI Research Department of Agere Systems in Holmdel. He was a co-recipient of the 1998 IEEE Journal of Solid-State Best Paper Award for a paper on a color digital CMOS camera.

WIDEBAND AMPLIFIERS



Amplifiers used in fiber optic receivers and transmitters must satisfy a wide range of requirements. The design challenges are compounded by packaging, power supply and interface aspects. The opto-electronic devices that the chips are coupled with are examined and system requirements are translated into circuit specifications such as bandwidth, dynamic range, group delay and drive capability. The design of a 10Gb/s driver for uncooled laser applications serves as an example.

Instructor: Hans Ransijn received the EE Degree from Delft Univ. of Technology, Netherlands in 1982. He co-founded a semi-custom IC design house DICE (Delft Integrated Circuit Engineering) and worked as a Technical Staff Member with the CATV department of the Dutch PTT in 1983. From 1983-1985 he was with the Space Research Organization Netherlands (SRON), where he designed analog front ends for space-borne instrumentation. In 1985 he joined AT&T Bell Labs in Reading, PA, now Agere Systems, where he is working on high-speed physical-layer circuits for 10 and 40Gb/s fiber-optic communication systems.

CHIP-TO-CHIP COMMUNICATION



Chip-to-chip I/O performance is projected to exceed Tb/s of aggregate bandwidth. Serious circuit design issues emerge in building low area, high-speed (multi-Gb/s), low power, and noise robust I/O busses. Designs of transmitters and receivers for parallel I/O busses are described emphasizing low-cost design techniques to achieve low jitter and high signal integrity (noise filtering and equalization).

Instructor: C.K. Ken Yang received BS and PhD in EE from Stanford Univ. in 1992 and 1998, respectively. He joined Rambus Inc. during a leave of absence for one year in 1993 to design a 500MB/s memory interface on a 16Mb DRAM. In 1999, he joined the UCLA Dept. of EE as an Assistant Professor. His research on high-performance mixed-mode circuit design primarily focuses on high-speed clock and data recovery for large VLSI systems.

CLOCK AND DATA RECOVERY FOR SERIAL DATA COMMUNICATIONS

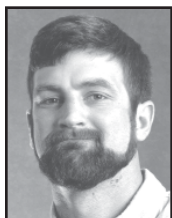


Techniques for data transmission over serial optical and electrical links are presented with the common distortions that occur over such links. Topics including eye diagrams, jitter tolerance, jitter transfer function, and jitter generation are introduced along with data encoding for run length control, framing, and DC-balance. The talk describes monolithic clock recovery emphasizing bang-bang PLL design and components such as data-driven phase/frequency detectors, charge pumps, ring oscillators, and multi-phase sampling structures.

Instructor: Richard Walker received BS in Engineering and Applied Science from the California Institute of Technology in 1982, and MS in Computer Science from California State Univ., Chico, CA in 1992. Rick joined Agilent Labs (formerly Hewlett-Packard) in 1981, where he is currently a Principal Project Engineer. His interests include broadband-cable modem design, solid-state laser characterization, bang-bang phase-locked-loop theory, 64b/66b 10GbE linecode design, and gigabit-rate serial data transmission. He holds 13 US patents.

Tutorials

Specifications and Figures of Merit for Mixed-Signal Circuits— A Guide to Understanding Where the Numbers Come from and What They Mean



This tutorial explores specifications of mixed-signal circuits featured at ISSCC. An overview is provided of what the specification means, what makes the specification important for a given circuit, what is easy and what is difficult, and what to watch for when specs are quoted. Different “Figures of Merit” (where specifications are combined) are considered. Performance benchmarks from past (and present) ISSCCs are provided. Specifications of A/D converters, D/A converters, amplifiers, filters, VCOs and phase-locked loops are discussed.

Instructor: David Robertson is Product Line Director of the High Speed Converter Group at Analog Devices, Inc. He received BA and BE from Dartmouth College, in 1984 and 1985 respectively, and since 1985 has worked at Analog Devices as a design and product engineer on a wide variety of D/A and A/D converters on complementary bipolar, BiCMOS and CMOS processes. He holds 14 patents on converter and mixed-signal circuits, has participated in two Best Panel ISSCC Evening Panel Sessions, and is co-author of a paper that received the JSSC 1997 Best Paper Award.

Design for Reliability in CMOS VLSI



As VLSI continues to scale, the likelihood of chip failure increases dramatically. At the same time, consumers expect electronic systems will be increasingly reliable. Rather than being confined to technical conferences and publications, reliability failures of high-profile computer systems now make headline news. This tutorial reviews the most common failure mechanisms and terms used to describe them. It describes three categories of reliability: (1) hard failures such as electromigration and gate-oxide breakdown, (2) soft failures induced by alpha particles and cosmic ray neutron hits, and (3) circuit failures caused by mechanisms such as leakage sensitivity and thermal hot spots. For each of these failure mechanisms, strategies are considered for analysis and design-around.

Instructor: David Greenhill is Senior Engineer of Sun Microsystems UltraSparc design team in Sunnyvale, CA. In 1986, he graduated from Imperial College, London, with Physics BSc. From 1986 to 1992, he worked for INMOS in Bristol, England, on CMOS VLSI design, color look-up tables, video controllers, and transputer microprocessor design. He joined Sun Microsystems in 1992 and worked on the UltraSparcI and UltraSparcII designs. He is currently Chief Engineer for the implementation of UltraSparcV. His interests include high-performance CMOS circuit design and technology, CAD and reliability of high-performance multiprocessor computer systems. He is involved in circuit analysis and design tradeoffs for reliability in these systems. He has been a member of the ISSCC Program Committee since 1997.

High-Dynamic-Range Image Sensors



This tutorial provides a framework for analyzing performance of image sensor dynamic range (DR) extension techniques and for comparing their effectiveness. A brief introduction to conventional image sensors, such as CCDs, CMOS APS and DPS is provided. A model is given for the signal path through an image sensor from input photocurrent to output voltage, including signal integration, dark current, temporal noise, and FPN. The model is used to define DR and SNR. Techniques for extending image sensor DR, including well-capacity adjusting, spatially-varying pixel exposure, time to saturation, and multiple capture are described. These techniques are compared, based on SNR. As DR is extended, some of these techniques suffer from higher loss in SNR than others, which limits their effective DR extension. Comparisons based on other criteria such as spatial resolution and implementation complexity are discussed. Other types of high-DR sensors, e.g., logarithmic sensors and silicon retina, are discussed. Recent research in the area is covered.

Instructor: Abbas El Gamal received BS EE from Cairo Univ. in 1972, MS in statistics and PhD in EE from Stanford in 1977 and 1978, respectively. From 78-80 he was Asst. Prof. of EE at Univ. of Southern California. He joined Stanford in 1981, where he is now Prof. of EE. From 1984-8, on leave from Stanford, he was Director of LSI Logic Research Lab, cofounder and Chief Scientist of Actel. From 1990-1995 he was a cofounder and Chief Technical Officer of Silicon Architects (now part of Synopsys). He is principal investigator on the Stanford Programmable Digital Camera Project. His research interests include: CMOS image sensors and digital camera design, image processing, network information theory, and electrically-configurable VLSI design and CAD. He has authored or coauthored over 100 papers and 25 patents in these areas. He serves on the board of directors and advisory boards of several IC and CAD companies. He is Fellow of the IEEE and member of the ISSCC Program Committee.

Ferroelectric Memory Design (FeRAM 101)



FeRAMs are nonvolatile memories that compete favorably today with EEPROMs and Flash memories in terms of write speed and power consumption. This tutorial covers the basics of ferroelectric materials, ferroelectric capacitors as circuit elements, ferroelectric memory cell circuits and their read/write operations, reference generation, and FeRAM architectures.

Instructor: Ali Sheikholeslami is an Asst. Prof. of ECE at the Univ. of Toronto. His research interests are VLSI memory design (including SRAM, DRAM, and content-addressable memories), ferroelectric memory design (circuit design and modeling), multiple-valued memories, and high-speed signaling. He has several journal and conference papers and two US patents in the area of ferroelectric memories.

Architectures and Design Methods for Cryptography



As electronic systems evolve from centralized to distributed, communicating devices, the need for security and encryption grows. This tutorial introduces the basics of cryptographic algorithms, the specialized mathematics involved, and the protocols commonly used today (e.g., SSL and IPsec). The tutorial then maps the various functions and protocols to VLSI architectures and describes different implementation techniques.

Instructor: Ingrid Verbauwhede, Univ. of California, Los Angeles, received PhD from K. U. Leuven, Belgium in 1991. From 1992-1994, she was visiting post-doc researcher at U.C. Berkeley. From 1994 to 1998, she was Principal Engineer at TCSI and ATMEL, and in 1998, joined UCLA as Assoc. Prof.. Her current interest is architecture design, design methods and VLSI implementation of specialized processors for wireless communication, networking and encryption.



Instructor: Jim Goodman, Lumic Electronics, Ottawa, Canada, received PhD from MIT in 2000, where his research focused on reconfigurable energy-efficient VLSI architectures for cryptography. From 2000 to 2001 he was Senior IC Architect at Chrysalis-ITS, developing next-generation network security processors. He is currently Senior Mixed Signal Architect at Lumic Electronics, developing low-power multimedia processors.

Introduction to Wireless-Receiver Design



An introduction to integrated receivers focuses on performance requirements for GSM cellular handset applications: (1) Overview of radio standards for sensitivity, blocking, AM suppression, and intermodulation. (2) Comparison of heterodyne, direct conversion, and low-IF receiver architectures. (3) Discussion of design specifications and tradeoffs.

Instructor: G. Tyson Tuttle, Silicon Labs, Austin TX holds an MS from UCLA and a BS from John Hopkins Univ., both in EE. He has held positions at Crystal Semiconductor and Broadcom Corp. focusing on high-speed mixed-signal circuit design for hard disk drive read channel and Ethernet applications. He joined Silicon Labs in 1997 where he is currently Product Manager for CMOS cellular wireless transceiver ICs. He holds 6 patents, is author or co-author of 6 technical publications, and is a member of IEEE.

CMOS Optical-Front-End Circuits



This tutorial provides analysis of CMOS integration techniques and their limitations for optical-front-end circuits: (1) Discussion of transimpedance amplifiers and their optimization for speed and sensitivity. (2) Description of decision networks for data-recovery and its problems. (3) Examples and implementations of CMOS Gb/s circuits.

Instructor: Michiel Steyaert received his PhD in Electronics from Katholieke Universiteit Leuven in 1987. In 1988 he was Visiting Asst. Prof. at the University of California, Los Angeles. From 1989-1996 he was NFWO Senior Research Associate at the ESAT Lab., K. U. Leuven, where he is now Professor. His research interests are high-frequency analog integrated circuits for high-frequency signal processing and for telecommunication circuits.

Workshop on Analog Telecom
IEEE Solid-State Circuits and Technology Committee
Sunday, February 3, 2002 - San Francisco Marriott Hotel
Organizer: Jan Sevenhans, Alcatel

The analog design community faces challenges of requirements for analog front-end building blocks such as high-voltage high-performance high-efficiency line drivers, high-resolution high-speed A/D and D/A converters, and upstream/downstream filters.

The major success of DSL technology worldwide places all telecom manufacturers under pressure for next-generation DSL products: increasing density of the lines per board, reducing power consumption per line and maximizing loop reach and robustness against disturbances such as RFI and bridge taps.

DMT signalling has opened golden gates on copper cable but leaves the system with a power bottleneck in the line drivers because of the high crest factor. Class A/B amplifiers, still in ADSL production lines, will soon be replaced with Class G, Class H, Class K and other high-efficiency power amplifier concepts re-invented today, going back to the future and remembering audio low-power high-efficiency concepts.

Loop-reach requirement push analog designers to achieve 14b-resolution A/D and D/A converters in high-volume-production highly-integrated analog front ends. Sigma-delta pipelined and various subranging architectures at the interface between analog and digital are revisited in advanced research programs. FDM upstream/downstream filtering is reconsidered to avoid carrier attenuation in the filter overlap region and the consequent loss of loop reach.

Speakers from telecom and silicon industry and from university research centers bring attendees up to date on the analog challenges of this emerging access application.

<u>Topics</u>	<u>Time</u>
Welcome & Introduction	8:30-8:45
Trade Offs in ADSL Analog Front-End Requirements Peter Reusens, Alcatel, Antwerp, Belgium	8:45-9:30
Analog Design Challenges in ADSL Filter and Low-Noise Circuits Samuel Sheng, LSI Logic, San Jose, CA	9:30-10:15
BREAK	15 min
ADSL Transceivers : Optimizing Power, Cost, Function and Performance Russell Apfel, Legerity, Austin, TX	10:30-11:15
ADSL Line Transceivers, Power and RX Integration Trends Marco Corsi, Texas Instruments, Dallas, TX	11:15-12:00
LUNCH	12:00-2:00
Silicon Technologies and Circuit Topologies for High Efficiency in ADSL Line Drivers Domenico Rossi, STMicroelectronics, Agrate, Italy	2:00-2:45
Line Drivers for xDSL Tim Piessens, K.U. Leuven, Leuven, Belgium	2:45-3:30
AFE Design for VDSL: a Case Study Joerg Hauptman, Infineon, Villach, Austria	3:30-4:15
BREAK	15 min
Concluding panel: DSL Analog Strategy of the Future	4:30-5:30
Conclusion	5:30

ISSCC Microprocessor Design Workshop**Thursday, February 7th, 2002** - San Francisco Marriott Hotel**Organizing Committee:** Sam Naffziger (Chair), Hewlett Packard; John Maneatis, True Circuits, Inc.; Kerry Bernstein, IBM
Ron, Preston, Intel; Simon Segars, ARM; Hector Sanchez, Motorola; Ian Young, Intel

This year, the Workshop addresses issues of high-frequency clocking on a variety of levels: architecture, circuit, process technology, and chip to chip interconnection.

As frequencies have driven relentlessly up into the multi-GHz range, the problem of getting that multi-GHz clock to all parts of the chip has become increasingly difficult. This Workshop seeks to enable designers of next generation processors to deal effectively with these difficulties by addressing the following issues:

Clock partitioning: As processor complexity grows, the span of the clock must increase to cover all the additional circuitry. When combined with larger wire delays and increased variability, many processor architects are looking at ways to partition the design into smaller quanta, each of which can operate in its own, somewhat independent clock domain. Topic 3 examines some of these tradeoffs.

Asynchronous methods: One solution to distributing the high frequency global clock is to eliminate it by resorting to largely asynchronous circuit implementations. Some of the methods of design and analysis of such systems are presented in topic 5.

Process variability: As transistor and interconnect geometries continue to shrink, designers are faced with the increased impacts of not only wire RC delays, but the increased variability of these wires and circuits. The net result is that it is much harder to reliably deliver a synchronous clock to all corners of the die. Topics 2, 6 and 7 seek to enable designers to analyze and understand this variability and deal with the implications for clock distribution.

Skew management: The increased uncertainty in actual clock arrival time across the chip has resulted in designers seeking out new ways to either reduce the clock skew with active circuitry or make the clocked storage elements less sensitive to the effects of skew. Some of these approaches are discussed under topics 4 and 7.

The workshop wraps up with representatives from both academia and industry painting pictures of what it will take to produce and consume reliable clocks for 10 to 20GHz processors. The path to achieving those clock frequencies in the next few years will certainly traverse many of the methods discussed in this workshop.

Workshop Introduction and Overview of Clocking Sam Naffziger, Hewlett-Packard	8:30
Process Technology Scaling Trends Krishna Saraswat, Stanford University	9:00
BREAK	9:45
Clocking Impacts on Architecture - future directions Matt Reilly (Intel)	10:00
Design of Sequential Elements Vojin Oklobdzija (University of California, Davis)	11:00
LUNCH	12:00
Clock tolerant architectures - Asynchronous methods and issues Simon Moore, Cambridge University	1:00
Manufacturing components of delay variation Sani Nasif (IBM)	2:00
Clock skew components and methodologies for analysis and design David Harris, Harvey Mudd College	2:30
BREAK	3:30
i) Clocking solutions for 10-20GHz processors Tom Chen, Colorado State University	3:45
ii) Architecture implications for Clocking in 10-20GHz processors Dave Sager, Intel	4:15
Workshop Discussion, All speakers	4:45
Conclusion	5:15

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ISSCC 2003 Call for Papers

IEEE International Solid-State Circuits Conference



**Sunday -Thursday, February 9-13, 2003,
San Francisco Marriott Hotel, San Francisco, CA**

Original papers are solicited in subject areas including, but not limited to, the following:

ANALOG — amplifiers; dc-dc converters; continuous-time & discrete-time filters; comparators; multipliers; voltage references; sample-and-hold circuits; Nyquist-rate & oversampling A/D and D/A converters; power-control circuits; consumer electronics; non-linear analog circuits, opamps, switched-capacitor circuits.

WIRELESS & RF COMMUNICATIONS — transceiver circuits and subcircuits for RF/IF/baseband; wireless LAN, Bluetooth, GSM/EDGE/CDMA/UMTS/3G basestation/handsets, TV/Radio/Satellite, DVB, HDTV, MMDS; active antennas, RF MEMS, RF power amplifiers, LNAs, mixers, oscillators, frequency synthesizers, phase-locked loops.

WIRES — LAN; WAN; FDDI; Ethernet; token ring; Fiber Channel, SONET; ATM; ISDN; xDSL; cable-modem and broadband communication over cable; optical data links, power-line/phone-line home networks; subscriber-line circuits, modems; oscillators.

DIGITAL — design, fabrication, and test of digital VLSI systems; microprocessors and network processors; I/O and inter-chip communication; intra-chip communication; reconfigurable logic arrays; clock synthesis and architectures; high-performance and low-power logic-micro-architecture and transistor-circuit techniques; high-speed FET and Bipolar digital circuits.

IMAGERS, DISPLAYS & MEMS — image sensors and related imaging techniques; smart sensors; integrated sensors and transducers; display drivers and controllers; thin-film-transistor interface circuits; organic LED and liquid-crystal-display interface circuits; flat-panel and projection displays; biosensors; sensor-interface circuits; sensors for medical applications; optical MEMS, MEMS for sensor and instrumentation applications.

MEMORY — design, fabrication, and test of static and dynamic memories; memory architectures; redundancy techniques and self-test; nonvolatile and read-only memory; Floating-gate, Ferro-Electric, Magnetic, and other novel structures; application-specific and embedded memories; low-power memory systems.

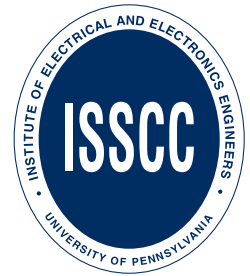
SIGNAL PROCESSING — digital & analog signal processors and cores; video and graphic processors; reconfigurable signal-processing circuits; magnetic and optical storage circuits; HDTV; image and voice-band processing/compression; multimedia circuits; communication processors; cryptographic and security processors; system-on-a-chip design methodologies and platforms.

TECHNOLOGY DIRECTIONS — advanced circuit technologies and techniques: deep-submicron technologies, compound semiconductors; superconductivity, photonics, nanoelectronics, 3D-electronics, technologies for bio-medical and microfluidic applications; organic electronics; coatable electronics; low-voltage/low-power techniques; high-performance mixed-signal and RF circuits, on-chip passive RF components; microprocessor architectures and design methodologies; analog processors; advanced memories, optical processors and backplanes, neural processors, fuzzy logic, multi-valued logic.

A submission may be accepted as either a regular paper or a short paper. A regular paper is allowed 23 minutes for presentation and 7 minutes for questions. Short papers are allowed 15 minutes total for both presentation and questions. Regular and short papers have the same submission requirements and quality standards. They differ only in the determination by the Program Committee of the time required to present the key ideas. Companion papers for large chips that require two paper slots to discuss both architecture and circuit details are encouraged.

2003 Conference Theme: "Power-Aware Systems"

Submission Deadline is Wednesday, September 4, 2002



ISSCC 2003 Call for Papers

Sunday - Thursday, February 9 - 13, 2003
San Francisco Marriott Hotel, San Francisco, CA

The 2003 Conference theme is "Power-Aware Systems." Papers describing ICs targeted for computing, telecommunication, and multimedia systems in all of the listed areas are solicited. Examples include high-performance microprocessors and memories, advanced telecommunication and data-communication ICs, imagers, and MEMs, analog circuits, and signal-processing ICs. Note that a technical co-operation has been initiated between SSCS/ISSCC and the Design Automation Conference (www.dac.com). A similar co-operation has also been initiated with the Non-Volatile Semiconductor Memory Workshop. Authors of papers directed at these technical events doing work relevant to ISSCC are encouraged to submit circuit-related papers.

Submission of Abstract, Draft Manuscript and Supplementary Material

Authors should submit 3 items for review: 1) An **Abstract** to be used in the Advance Program, 2) A **Draft** of the final **Manuscript** for the Digest of Technical Papers, 3) Additional **Supplementary Material**, which is not mandatory but strongly encouraged. To submit a paper, you must go to <http://www.isscc.org/isscc> on the WEB and complete the requested information. This will include the paper title, contact-author information, other authors, abstract, suggested review area, and a number of questions regarding your electronic format. **Draft manuscript and supplementary material must also be submitted electronically to the WEB site. This WEB site will be available for submissions by July 1, 2002, although you may consult the WEB site for instructions at any time.** Authors are encouraged to complete the WEB site questions early. Your information can be updated anytime up to the September 4, 2002 deadline. A sample Digest Paper and Abstract can be found at the WEB site. If you do not have WEB access, and would like to submit a paper, contact Courtesy Associates: Tel: 202-973-8667, Email: isscc@courtesyassoc.com.

1. The **Abstract** must be submitted to the ISSCC WEB site (<http://www.isscc.org/isscc>). The abstract must not exceed 325 characters. ISSCC reserves the right to edit the title and the abstract to accommodate the program format. The abstract must be factual and provide as complete a description as possible, including specific quantified performance data. Claims such as "new," "advanced," "novel," "high-performance," and "high-speed" are not acceptable.
2. The **Draft-Manuscript** text and figures must be submitted electronically to the WEB site (<http://www.isscc.org/isscc>). The text must contain all essential information, including references to previously published work. It must have a minimum of 5200 characters, and must not exceed 7200 characters. Six figures are allowed in addition to a die micrograph. A range of formats will be accepted for the electronic draft-manuscript submission. Refer to the WEB site for details. Authors of accepted papers will have an opportunity to revise their drafts. The Program Committee may require specific revisions.
3. **Supplementary Material** must also be submitted electronically through the WEB site (<http://www.isscc.org/isscc>). It must be supplied as an attachment to, but separate from, the draft manuscript. It must not exceed 10 pages. This material should contain information that will help the Program Committee in its decisions. Examples are copies of additional figures to be shown as visuals, additional text explaining key points in more detail, and a clear review of how the work described extends the previous state of the art, and documentation of prior publication.

The most common reason for paper rejection is a lack of clear evidence of what is novel in the work and the extent to which it advances the state of the art. Successful submissions contain specific new results, sufficient detail and data to be understood, and schematics and measured results for key circuits when appropriate.

Supplementary material must also state clearly what, if anything, will have been published prior to the Conference. Copies of these prior publications should be submitted, including data sheets, press releases, and other forms of publication.

In addition to electronic draft-manuscript submission, authors must submit two verification hard copies of the draft manuscript and any supplementary material by overnight courier to the US address provided on the WEB site. The WEB site will provide the mailing address for hard copy submission.

All materials submitted in paper form must be prepared in single-sided, double-spaced form. **Each copy must include, as the first page a copy of the Abstract as printed from the WEB site.** This Abstract page will contain your paper number, title, contact information, list of authors, suggested topic area, and the text of the abstract. Each submitted copy must have, **stapled as a single unit**, the Abstract page, the Draft-Manuscript, and any Supplementary Material provided.

Confirmation of paper (hard copies) receipt: Authors will receive an email or fax with their name, paper title, and submission number for confirmation of receipt of the hard copy of their paper. This is the only confirmation that will be sent.

For further details on manuscript preparation, check the Conference WEB site at <http://www.isscc.org/isscc>, or send an Email with your questions to ISSCC@courtesyassoc.com.

POLICY REGARDING PAPER-SUBMISSION DEADLINE

Due to the timing constraints associated with the paper-review process, papers must be received by the deadline shown below to be considered by the Program Committee. Use of EXPRESS DELIVERY SERVICE is required for traceability. Papers received after the deadline will be returned to authors unopened.

“Hard” Deadline for Receipt of Paper: Wednesday, September 4, 2002

WEB-based Submission of Final Manuscript

The author(s) of accepted papers will submit via the WEB by November 1, 2002, a final, illustrated version for publication in the ISSCC Digest of Technical Papers. The preferred text-submission format is Word. However, Framemaker, Latex, and others that generate .rtf files are acceptable. The length limit (between 5200 and 7200 characters) will be strictly enforced electronically. Papers exceeding the length limit will be immediately rejected, as requiring length editing. **The preferred figure format is PowerPoint.** However, Freelance, PDF, & PostScript can be accommodated if needed. A 6-figures-plus-die-photo maximum will be enforced. Figures 2a and 2b count as two figures! Tables count, and are labeled, as figures. For instructions see <http://www.isscc.org/isscc>. At the Conference, all visuals will be converted to PDF for electronic projection.

Clarification of Pre-Publication and Press-Coverage Policies

The Conference pre-publication policy is intended to maintain ISSCC as the premier global forum for debut of technical innovation in such areas as architecture, circuitry, and algorithms. Contrary to popular opinion, a paper may be acceptable even if it is connected with a product that has sampled, entered production, and/or appeared in a publication. In such situations, the Program Committee is responsible for assessing whether substantial technical disclosure has already taken place. The substantial-technical-disclosure rule may be complied with even if there has been disclosure of: abbreviated data sheets that provide only specifications, a feature list, and coarse block diagram; material under nondisclosure agreement; die photos; articles addressing only the marketing or applications aspects of the product; presentations at workshops or niche conferences with limited attendance and **no** published proceedings or press coverage. Conversely, a paper will be rejected if disclosure of the innovative circuitry, architectures, algorithms, etc. occurs in articles, data sheets, trade journals, or other conferences. **Detailed disclosure of innovative technical ideas on the World Wide Web will be considered pre-publication.** Prospective authors should submit all material relevant to pre-publication at the time of paper submission. Abstracts of accepted papers will be disclosed to the press in November. The ISSCC reserves the right to add factual information to the abstract from the paper text, and to modify the paper title when technically appropriate. Copies of final manuscripts, including figures, will be made available to approved members of the press prior to the Conference for post-Conference articles.

For further details on pre-publication policy, or assistance in assigning a subject area, contact the Program-Committee Chair: Anantha Chandrakasan, Tel: 617-258-7619, Fax: 617-253-5053, Email: anantha@mtl.mit.edu

Limited financial assistance is available to student presenters upon request.

ISSCC 2003

Sunday - Thursday
FEBRUARY 9 - 13, 2003
SAN FRANCISCO MARRIOTT HOTEL, SAN FRANCISCO, CA

ISSCC 2003 CALL FOR PAPERS
PLEASE CIRCULATE/POST ON BULLETIN BOARD
SAN FRANCISCO MARRIOTT, SAN FRANCISCO, CA / FEBRUARY 9 - 13, 2003

The Solid-State Circuits Society
of the IEEE
C/O JS McCarthy Printers
15 Darin Drive
Augusta, ME 04330
USA

If you need technical assistance, please contact the appropriate Subcommittee Chair or Secretary.

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For further details on pre-publication policy, or assistance in selecting a subject area, contact:

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For further author information see the Conference Website: <http://www.isscc.org/isscc> or contact Courtesy Associates.

“Hard” Deadline for Receipt of Paper (2 hard copies): Wednesday, September 4, 2002

TIMETABLE OF ISSCC 2002 SESSIONS

Sunday, February 3rd

ISSCC 2002 TUTORIALS

8:00 AM	T1: Specifications and Figures of Merit for Mixed-Signal Circuits T2: Design for Reliability in CMOS VLSI T3: High-Dynamic-Range Image Sensors T4: Ferroelectric-Memory Design (FeRAM 101)	T5: Architectures and Design Methods for Cryptography T6: Introduction to Wireless-Receiver Design T7: CMOS Optical-Front-End Circuits
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SSCTC WORKSHOP

8:30 AM	SSCTC Workshop on Analog Telecom-Access Circuits and Concepts (Salon 7)
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SPECIAL TOPIC EVENING SESSIONS: NEXT-GENERATION CIRCUIT-DESIGN CHALLENGES

7:30 PM	SE1: Inductance: Implications and Solutions for High-Speed Digital Circuits (Salon 1-6)	SE2: Low-Voltage Design for Portable Systems (Salon 7)
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Monday, February 4th

ISSCC 2002 PAPER SESSIONS

8:30 AM	Session 1: Plenary Session (Salons 7-9)				
1:30 PM	Session 2: Image Sensors (Salon 1-6)	Session 3: Digital Signal Processors, Circuits and Systems (Salon 7)	Session 4: Backplane Interconnect (Salon 8)	Session 5: Wireless-Networking Transceivers (Salon 9)	Session 6: Non-Volatile Memories and SRAM (Salon 10-15)
5:00 PM	Author Interviews and Social Hour (Golden Gate Hall)				

ISSCC 2002 DISCUSSION SESSIONS

8:00 PM	E1: Software Radio: Cool or to be Cooled? (Salon 1-6)	E2: When Will Optical Interconnects Appear on High-Performance Microprocessors? (Salon 7)	E3: Does Moore's Law Apply to Analog? (Salon 8)	E4: Have Universities Killed Research or Has Industry Corrupted It? (Salon 9)
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Tuesday, February 5th

ISSCC 2002 PAPER SESSIONS

8:30 AM	Session 7: Baseband Communications (Salon 1-6)	Session 8: High-Speed Timing (Salon 7)	Session 9: DRAM and Ferroelectric Memories (Salon 8)	Session 10: High-Speed ADCs (Salon 9)	Session 11: TD: RF/High-Speed Technologies (Salon 10-15)
1:30 PM	Session 12: TD: Digital Directions (Salon 1-6)	Session 13: Oversampling A/D Converters (Salon 7)	Session 14: Cellular RF Wireless (Salon 8)	Session 15: Gigabit Communications (Salon 9)	Session 16: High-Speed Circuit Techniques and I/O (Salon 10-15)
5:15 PM	Author Interviews (Golden Gate Hall)				

ISSCC 2002 DISCUSSION SESSIONS

8:00 PM	E5: Low-Voltage Design or the End of MOSFET Scaling? (Salon 1-6)	E6: $\Sigma\Delta$: Solution or Indigestion? (Salon 7)	E7: What Caused the Telecom Crash ? (Salon 8)	E8: Solid-State Circuits: System or Circuit Innovation? (Salon 9)
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Wednesday, February 6th

ISSCC 2002 PAPER SESSIONS

8:30 AM	Session 17: Advanced RF Techniques (Salon 1-6)	Session 18: Converter Techniques (Salon 7)	Session 19: DSL and Wireline Circuits (Salon 8)	Session 20: Microprocessors (Salon 9)	Session 21: TD: Sensors and Microsystems (Salon 10-15)
1:30 PM	Session 22: Multimedia Signal Processing (Salon 1-6)	Session 23: Analog Techniques (Salon 7)	Session 24: RF Systems (Salon 8)	Session 25: Processor Building Blocks (Salon 9)	Session 26: MEMS and Displays (Salon 10-15)
5:15 PM	Author Interviews (Ballroom Foyer South)				

Thursday, February 7th

ISSCC 2002 SHORT COURSE

8:00 AM	ISSCC 2002 Short Course: Wideband Communications (Sessions at 8:00 AM, 10:00 AM, and 1:30 PM) (Salons 1-6, Nob Hill, Golden Gate A)
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ISSCC 2002 MICROPROCESSOR DESIGN WORKSHOP

8:00 AM	Microprocessor Design Workshop (Salon 7)
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RECAPITULATIONS



This, the year-2002 edition of the ISSCC Visuals Supplement (formerly called the Slide Supplement), marks the thirteenth appearance of this novel product in conference documentation. It was first provided at ISSCC90, twelve years ago, following a conceptualization process begun only a few months earlier.

The acceptance of the first edition was sufficiently strong that we were encouraged to continue the logical development of the original concept. The result is open before you now. This year, again, it has been provided to every full registrant at ISSCC as part of their registration package, with world-wide delivery by priority or global mail, for expected arrival within three weeks of the end of the Conference.

While the basic idea remains the same – to provide a record of what was actually presented at ISSCC, very shortly after the close of the Conference - the mechanisms have varied in detail over the years. This year, the experiment in electronic projection introduced in three sessions in 2000 and extended to the full Conference in 2001 last year, was further extended to include all 174 papers plus the new Special-Topic Evening Sessions introduced at the Conference this year.

To facilitate the visuals-presentation and visuals-documentation processes, all speakers were requested to send hard and soft copies of their presentation a week before the Conference. For Speaker Rehearsal, each presentation was converted from the received format to PDF, to ensure consistency and quality of projection. The paper copies provided were used to check for aberrances in the code-conversion process, and to facilitate communication of the changes inevitably required by some speakers. For the majority, which were originated in Powerpoint, very little difficulty was found.

In the checking process introduced last year, each speaker was given a CD containing the presentation, for initial review and verification at Speaker Rehearsal. Then, following last-minute changes initiated by the Session Chair or speaker, a full-session PDF version was loaded on CD-ROM for back-up. The actual presentation was run from hard disc on two laptops, driving a common display, one system providing the back up for the other. As a result of the more-integrated process made possible by electronic projection, the quality of both the presentation visuals and the Visuals-Supplement pages has improved from earlier (“non-electronic”) years. Furthermore, problems encountered last year with those able to provide Framemaker or Latex were resolved by having them also provide a PDF version.

Of course, all of this virtually real-time process was possible only through the heroic cooperation of many many people: First and foremost, I must acknowledge the authors and speakers, who, almost without exception, graciously provided the requested hard-copy and soft-copy materials in a timely and effective fashion. Moreover, as a glimpse of the following pages will attest, the quality provided generally ranged from good to better than excellent. By and large, guidelines concerning line thickness, information density, and the like, were closely followed. As well, the electronic-processing procedure for book production introduced four years ago, and extended two years ago, continued to sustain a noteworthy quality standard in this final product.

Overall, a great deal of detailed work was necessary by a large number of volunteers, styled “The Saratoga Group” in recognition of the hotel meeting room in which the original Supplement was assembled. Each of these individuals, in a very special way, is deserving of our appreciation: To Sherif Abdalla, Steve Bonney, Ahmad Darabiha, Yadollah Eslami, Kamran Farzan, Warren Gross, Anas Hamoui, Shahriar Mirabbasi, Kostas Pagiamtzis, Jennifer Rodrigues, Saman Sadr, Kenneth Smith, Marcus van Ierssel, and Sarah Wood, must go our heartfelt appreciation for a job well and truly done, a job which occupied many of them virtually every waking hour for the best part of a week, and others for even more!

Finally, we wish to acknowledge the outstanding contribution of Richard Simmonds and his willing staff at the Business Center of the San Francisco Marriott Hotel. Many thanks to you all!

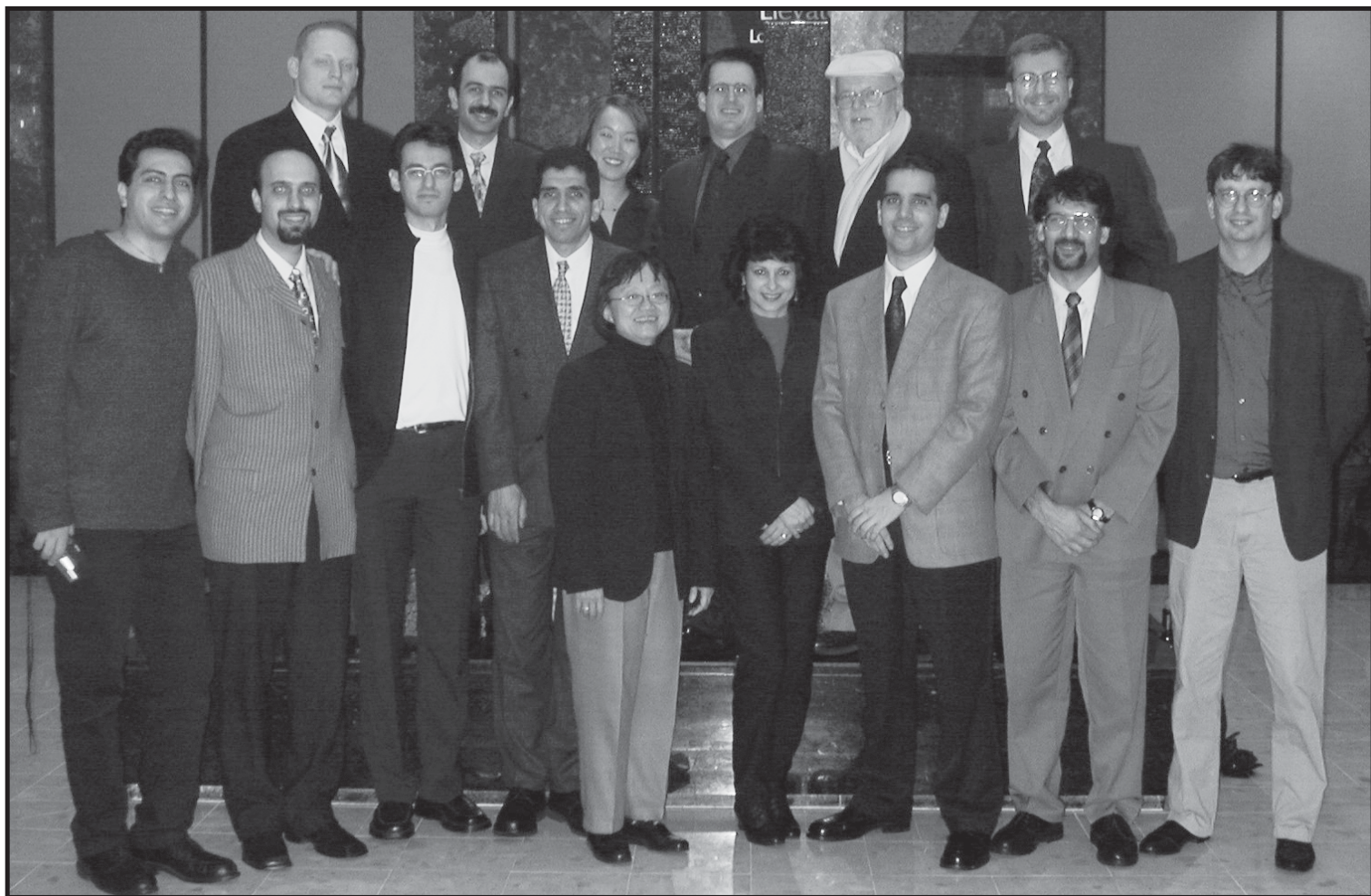
A handwritten signature in black ink, appearing to read 'L.C. Fujino' with a stylized flourish at the end.

Laura Chizuko Fujino
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2002 IEEE International Solid-State Circuits Conference

VISUALS SUPPLEMENT

Volume MMII
Visuals Supplement



Editor: Laura Chizuko Fujino

The Saratoga Group:

Sherif Abdalla, Steve Bonney, Ahmad Darabiha, Yadollah Eslami, Kamran Farzan, Warren Gross, Anas Hamoui, Shahriar Mirabbasi, Kostas Pagiamtzis, Jennifer Rodrigues, Saman Sadr, Kenneth Smith, Marcus van Ierssel, and Sarah Wood

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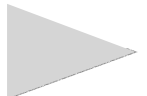
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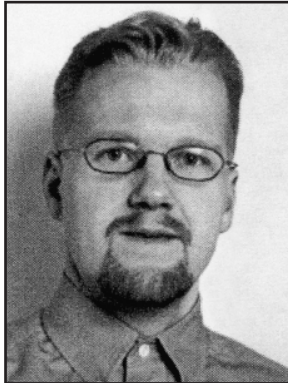




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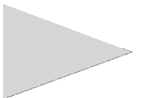
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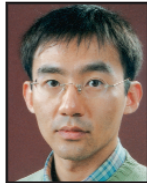


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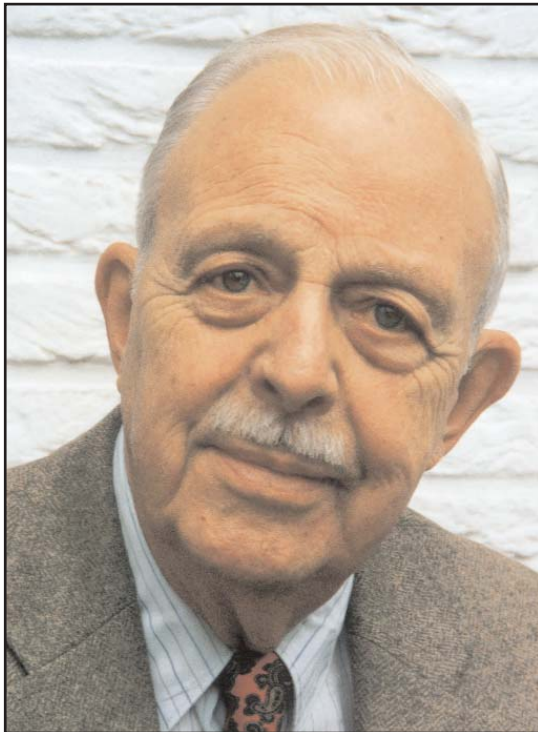
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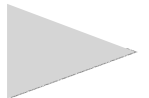
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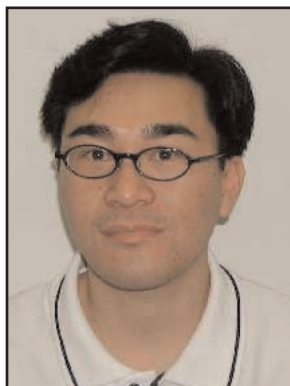




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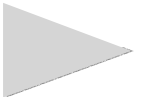
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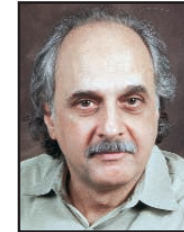
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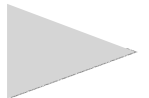
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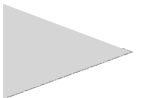
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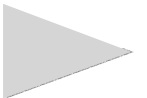


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for CONTRIBUTIONS to

high-speed A/D converters and mixed-signal integrated circuits.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS



Fellow Award

2002



Krishnaswamy Nagaraj

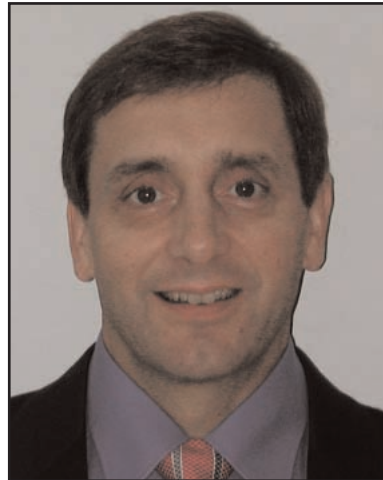
for CONTRIBUTIONS to
the design of CMOS data converters.

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Carl Matthew Sechen

for CONTRIBUTIONS to

automated placement and routing in integrated circuits.

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Jan Van der Spiegel

for CONTRIBUTIONS in

biologically motivated sensors
and information processing systems.

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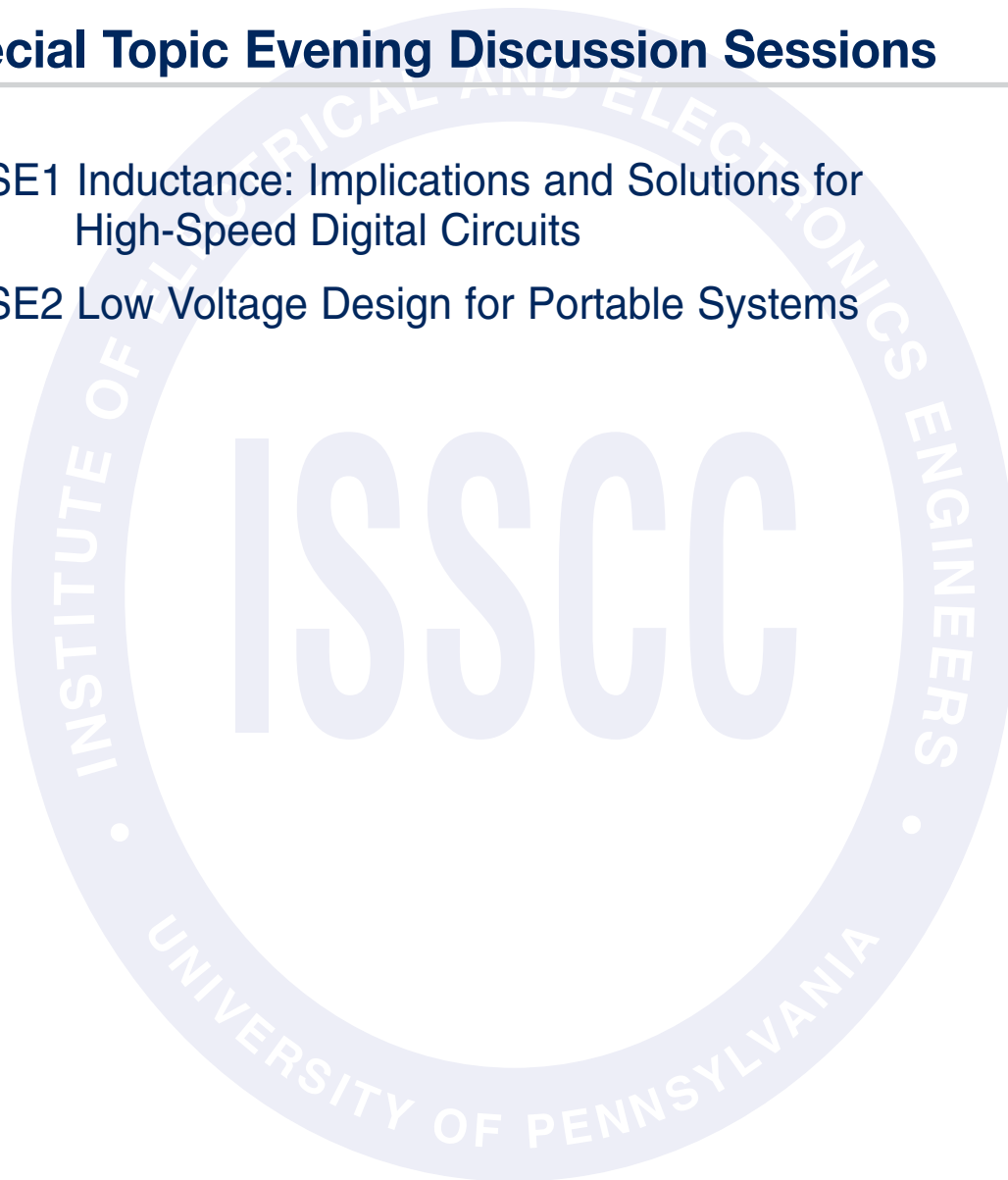


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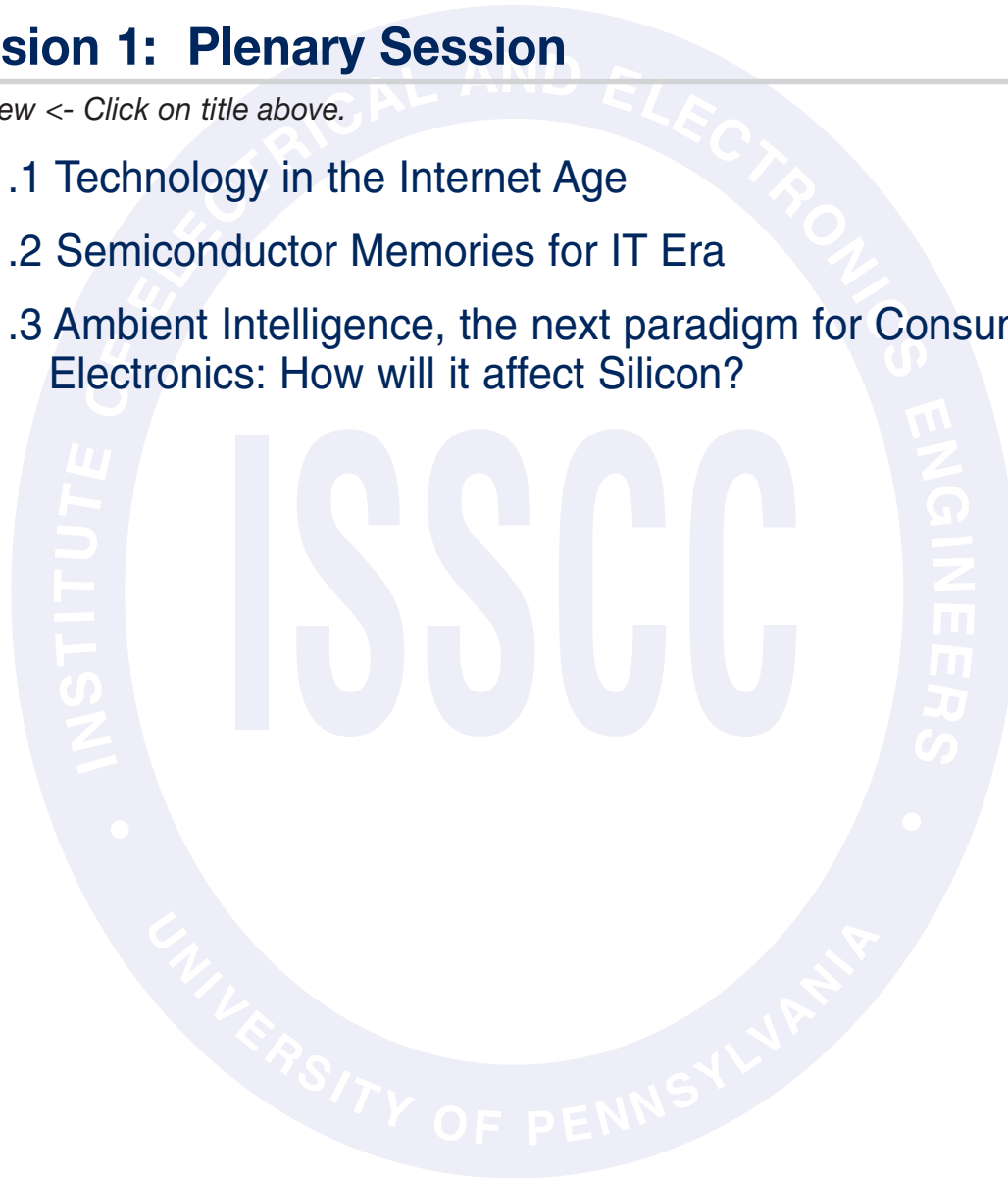
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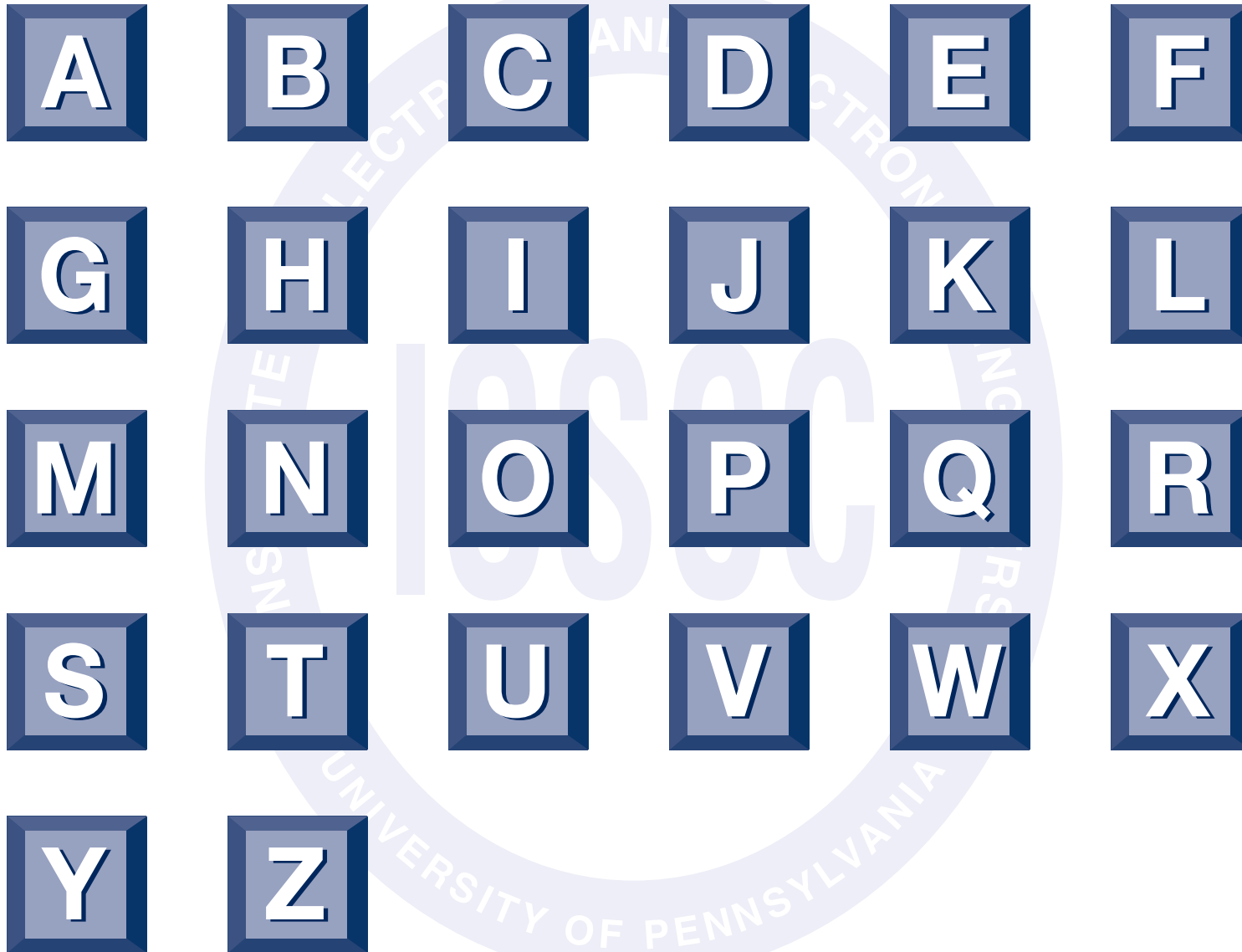
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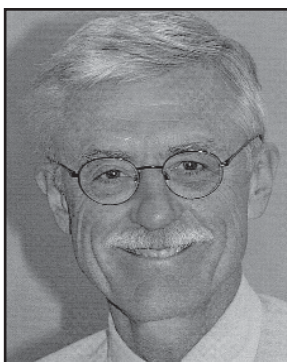
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D. Buss

1.1 Technology in the Internet Age

Dennis Buss

Texas Instruments, Dallas, Texas

Internet electronic products have requirements different from those of personal computers (PCs). The increasing importance of Internet electronics is driving changes in development of IC technology. One important characteristic of the Internet Age is computational disaggregation. Whereas, over the past 20 years, PCs have been characterized by ever-increasing computation capabilities, emerging Internet electronic products are characterized by sufficient computation to achieve the function in a small, often portable, form factor.

The imperative for lower cost, which enables penetration into mass markets, is a second area where Internet electronic products differ from PCs. Disaggregation and cost requirements are driving an unprecedented degree of system-on-a-chip (SoC) integration. In the Internet Age, SoC integration means more than integrating different digital cores. It also means integrating functions that are realized today in different technologies: logic, memory, analog, power management, passives and radio or wireline driver, depending on the product. Because SoC integration is motivated primarily by cost, diverse functions must be integrated together in standard CMOS with minimal cost addition.

Cost-effective embedded memory technology also needs to be developed. Current examples of SoC integration include cell phones, cable/DSL modems, and internet audio. These representative examples, together with others, are driving changes in the way ICs are developed. In the latter half of the decade, it is likely that SoC integration will expand to include MEMS, microphotonics, and on-chip energy sources. Moore's Law scaling will continue at least through the end of this decade, but SoC integration will become an increasingly important technology imperative for continued cost reduction throughout the Internet Age.

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C. G. Hwang

1.2 Semiconductor Memories for IT

C. G. Hwang

Samsung Electronics Co. Ltd., Yongin City, Kyunggi-Do, Korea

Information technology (IT) emerged from the 1970s based on main-frame computers. Since then, PCs and the Internet world have drastically expanded the IT industry along with rapid growth of network and communication technology. For almost all platforms, semiconductor memories have been a key enabling technology.

In the PC era, DRAM density increase has been driven by rapid expansion of applications with advanced operating systems. In the future, servers will continue driving high-density DRAM requirements, and the maximum memory size of servers will be one of the key performance parameters. 512Mb DRAM will be widely available in 2002 and 16Gb DRAM is expected to appear within the next 10 years.

Performance of semiconductor memories will be driven by graphics applications and network systems. 1Gb/s/pin DRAM will be popular in 2002 and 2Gb/s/pin in 2004 for high-end graphics applications. Random-access times in the range of 5ns for SRAM and 20ns for DRAM range and 1Gb/s/pin DRAM will be available in 2002, and even faster (frequency, latency) memories will be required for high-end network systems such as OC-768-based switches and routers and beyond.

Mobile platforms, especially 3G phones and PDAs, are driving low-voltage low-power memories. Standby power of DRAM and pseudo-SRAM has been reduced drastically over the last 2 years. 1.8V DRAM will be in volume production in 2002 and 1.0V DRAM is expected in 2005 for longer battery life and moving-picture capability of mobile applications. The small-form-factor requirement of mobile phones and consumer applications such as PDA, and DSC will expedite various multi-chip-package solutions such as SRAM+Flash, DRAM+Flash, and SRAM+DRAM+Flash. Recent digital convergence and the rapid reduction of \$/MB of mass storage flash memory increased the usage of flash memory in various mobile and consumer applications.

Semiconductor memory will continue to follow Moore's Law for at least the next 10 years and will be lead by mass storage flash memory technology. Memory requirement of various IT platforms will continue to increase the trend of MB/system and MB/person.

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F. Boekhorst

1.3 Ambient Intelligence: the Next Paradigm for Consumer Electronics: How Will it Affect Silicon?

Fred Boekhorst

Philips Research, Eindhoven, The Netherlands

Ambient Intelligence refers to an environment where the user experience is what matters. People want to have fun, feel free, enjoy life, feel secure, be in control and be productive. This experience is not linked to one particular device but is realized by a network of devices present in the environment that will provide us these experiences in an intelligent way.

Ambient Intelligence is introduced as a new paradigm in consumer electronics. Some of the technologies required for Ambient Intelligence are covered, with a focus on IC consequences. Ongoing work in three fields is described: ubiquitous radio, intuitive user/system interfaces and three-dimensional visual displays. These three fields highlight the diverse nature of Ambient Intelligence technologies as well as the resulting requirements for ICs. Considerations with respect to an introduction timeline of Ambient Intelligence are given.

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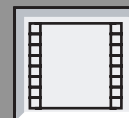
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L. Le Cam

2.1 A 1/1.8" 3M-pixel FT-CCD with On-Chip Horizontal Sub-Sampling for DSC Applications

Laurent Le Cam, Jan T. Bosiers, Agnes C. Kleimann, Harry C. van Kuijk, Joris P. Maas, Monique J. Beenhakkers, Herman L. Peek, Peter C. van de Rijt, Albert J. Theuwissen¹

Philips Semiconductors Image Sensors, Eindhoven, The Netherlands,
¹also with Delft University of Technology, Delft, The Netherlands

A 1/1.8" 3M-pixel frame-transfer CCD (FT-CCD) with on-chip horizontal sub-sampling allows an additional pre-view mode where the image extraction rate is doubled (up to 60 images/s) while keeping the 25MHz classic readout frequency. High-sensitivity video clips, fast auto-focus, and auto-exposure is achieved on digital still cameras.

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K. Yoon

2.2 Single-Chip CMOS Image Sensor for Mobile Applications

Kwangho Yoon, Chanki Kim, Bumha Lee*, Doyoung Lee

Hynix Semiconductor Inc, Ichon, Kyoungki, Korea, *National Semiconductor, USA

A CIF CMOS Image sensor contains fundamental color signal processing functions on-chip. The analog line memory, which can be accessed twice, enables simple color-interpolation and other signal processing in a small chip. At 30frames/s, the sensor consumes 20mW at 3.0V supply.

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R. Etienne-Cummings

2.3 A Single Chip for Imaging, Color Segmentation, Histogramming, and Pattern Matching

Ralph Etienne-Cummings^{1,2}, Philippe Pouliquen^{1,2}, M. Anthony Lewis¹

¹Iguana Robotics, Inc., Mahomet, IL, ²Dept. of ECE, Johns Hopkins University, Baltimore, MD

128(H)x64(V) x RGB CMOS imager is integrated with region-of-interest selection, RGB-to-HSI transformation, HSI-based pixel segmentation, 36-bins x 12b HSI histogramming, and sum-of-absolute-difference template matching. 32 learned color templates are stored and compared to each frame. At 30frames/s, it uses 1mW.

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D. Stoppa

2.4 138dB-Dynamic-Range CMOS Image Sensor with New Pixel Architecture

**David Stoppa, Andrea Simoni, Lorenzo Gonzo, Massimo Gottardi,
Gian-Franco Dalla Betta**

Istituto per la Ricerca Scientifica e Tecnologica (ITC/IRST), Povo, Italy

A 128x64 pixel image sensor in 0.35 μ m 3.3V CMOS technology achieves 138dB dynamic range by adapting single-pixel integration time to the local illumination conditions. Video frame rate is achieved with 0.2% rms temporal noise and 14mW power in a test chip.

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K. Kawajiri

2.5 1.5M Pixel Imager with Localized Hole Modulation Method

Takashi Miida, Kazuhiro Kawajiri, Hiroyuki Terakago, Tsutomu Endo, Tamotsu Okazaki, Shuji Yamamoto, Akitoshi Nishimura

Innotech Corporation, Yokohama, Kanagawa, Japan

A 1.5Mpixel imager with 4.2 μ m square pixel is composed of a single MOSFET and a pinned photo-diode. A localized high-density p-region near the source of MOSFET converts the accumulated hole number to source voltage. Low random noise, low dark signal, high sensitivity with good color reproduction and resolution are achieved.

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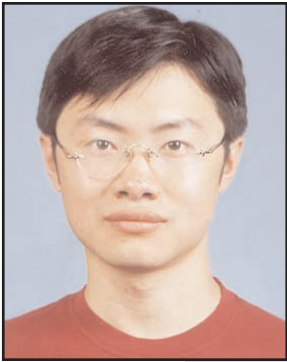


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C. Xu

2.6 A 1.0V V_{DD} CMOS Active Pixel Image Sensor with Complementary Pixel Architecture Fabricated with a $0.25\mu\text{m}$ CMOS Process

Chen Xu, Weiquan Zhang, Mansun Chan

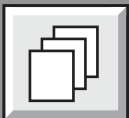
Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, HK

A 128x128 complementary CMOS active-pixel sensor (CAPS) is fabricated in $0.25\mu\text{m}$ CMOS for low-voltage application. A single-slope with correlated double sampling (CDS) is used in the readout circuit. The chip operates at a V_{DD} as low as 0.8V with 15dB added dynamic range compared with conventional CMOS APS.

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T. Goji Etoh

2.7 A CCD Image Sensor of 1Mframes/s for Continuous Image Capturing of 103 Frames

**T. Goji Etoh^{1,2}, D. Poggemann², A. Ruckelshausen², A. Theuwissen^{3,4},
G. Kreider³, H.-O. Folkerts³, H. Mutoh⁵, Y. Kondo⁶, H. Maruno⁶,
K. Takubo⁶, H. Soya⁶, K. Takehara¹, T. Okinaka¹, Y. Takano¹,
T. Reisinger^{1,2}, C. Lohmann^{1,2}**

¹Kinki University, Higashi-Osaka, Japan, ²University of Applied Sciences Osnabrück, Germany, ³Philips Semiconductors, The Netherlands, ⁴Delft University of Technology, The Netherlands, ⁵Link Research Corporation, Japan, ⁶Shimadzu Corporation, Japan

A single-chip CCD image sensor captures >100 successive images at >1Mframes/s. The pixel count of test chip is 312 x 260 (=81,120) pixels. Charge handling capacity is 40k electrons. Grey levels are 10b. Fill factor is 13%. On-chip overwriting mechanism makes possible continuous recording of the latest image signals, draining the old ones to the substrate.

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J. Hurwitz

2.8 A 35mm Film Format CMOS Image Sensor for Camera-Back Applications

**Jed Hurwitz, Mark J. Panaghiston, Keith M. Findlater,
Robert K. Henderson, Toby E.R. Bailey, Andrew J. Holmes,
Brian Paisley**

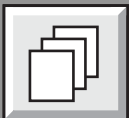
STMicroelectronics Imaging Division, Edinburgh, Scotland, UK

A 5V 1120x1808 pixel 35mm-film format CMOS image sensor for camera-back use, fabricated in 0.5 μ m 2P3M technology, includes integrated light-detection circuitry using non-destructive pixel read and consumes <math>50\muW. Reticle stitching is employed for the large format. Dynamic range is 66dB and peak SNR is 55dB.

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M. Lau

3.1 A Packet-Memory-Integrated 44Gb/s Switching Processor with a 10Gb Port and 12Gb Ports

**Michael Lau, Sam Shieh, Pei-Feng Wang, Brandon Smith,
Min-Shueh Yuan, Dennis Lee, James Gaba, Jason Chao,
Bernard Shung, Cheng-Chung Shih**

Broadcom Corporation, San Jose, CA

A 44Gb/s switching processor chip has 1MB embedded packet memory. With a 10Gb and 12 1Gb ports, this chip is useful for LAN/WAN bridging applications. Wirespeed switching performance is demonstrated using a shared buffer switching architecture. This 0.18 μ m CMOS processor integrates a 10Gb port with an XGMII interface.

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F. Lange

3.2 A 4.32GOPS 1W General-Purpose DSP with an Enhanced Instruction Set for Wireless Communication

Andreas Olofsson, Fredy Lange

Analog Devices DSP Design Center, Herzelia, Israel

A 6GOPS DSP implements the TigerSharc architecture with an instruction set enhanced for wireless communication. It is implemented in a 0.13 μ m process with 8 layers of copper interconnect and operates at 250MHz with 1W power dissipation under nominal conditions.

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S. Agarwala

3.3 A 600MHz VLIW DSP

Sanjive Agarwala, Peter Koeppen, Timothy Anderson, Anthony Hill, Michael Ales, Raguram Damodaran, Lewis Nardini, Paul Wiley, Steven Mullinnix, Jerald Leach, Anthony Lell, Michael Gill, Jeremiah Golston, David Hoyle, Arjun Rajagopal, Abhijeet Chachad, Manisha Agarwala, Roger Castille, Neil Common, John Apostol, Hasan Mahmood, Manjeri Krishnan, Duc Bui, Quang-Dieu An, Peter Groves, Luong Nguyen, N. S. Nagaraj, Ray Simar

Texas Instruments Inc., Dallas, TX

A 600MHz VLIW DSP delivers 4800MIPS, 2400 (16b) or 4800 (8b) million multiply accumulates at 0.3mW/MMAC (16b). The chip has 64M transistors and dissipates 718mW at 600MHz and 1.2V, and 200mW at 300MHz and 0.9V. It has an 8-way VLIW DSP core, a 2-level memory system, and 2.4GB/s I/O bandwidth.

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M. Miyazaki

3.4 A 175mV Multiply-Accumulate Unit Using an Adaptive Supply Voltage and Body Bias (ASB) Architecture

Masayuki Miyazaki^{1,2}, James Kao¹, Anantha P. Chandrakasan¹

¹Massachusetts Institute of Technology, Microsystems Technology Labs, Cambridge, MA, ²on leave from Hitachi Ltd., Central Research Lab

The power dissipation of a digital circuit is minimized by simultaneous control of power supply voltage and body bias. The technique minimizes power dissipation for varying processing rates through dynamic adjustment of V_{dd} and V_{bb} . A 16b MAC operates at 166kHz and 14nW at 175mV V_{dd} . A ring oscillator operates at 0.1V.

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J. Tierno

3.5 A 1.3GSample/s 10-Tap Full-Rate Variable Latency Self-Timed FIR Filter with Clocked Interfaces

Jose Tierno, Alexander Rylyakov, Sergey Rylov, Montek Singh¹, Paul Ampadu², Steven Nowick¹, Michael Immediato, Sudhir Gowda

IBM T. J. Watson Research Center, Yorktown Heights, NY, ¹Columbia University, New York, NY, ²Cornell University, Ithaca, NY

A 6b 10-tap digital FIR has a self-timed datapath, clocked interfaces, and variable latency. The 0.45mm² circuit in 0.18μm CMOS is operational from 1.2V to 2.1V power supply, and has 80mW dissipation at 300MSample/s and 4 cycles of latency, and 500mW at 1.3GSample/s and 7 cycles of latency.

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D. Redmond

3.6 A GSM/GPRS Mixed-Signal Baseband IC

David Redmond, Morgan Fitzgibbon, Alan Bannon, Darren Hobbs, Chunhe Zhao, Kiyoshi Kase, Joseph Chan, Michael Priel, Kevin Traylor, Keith Tilley

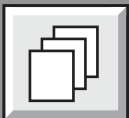
Motorola Inc., Cork Ireland, Phoenix AZ, Austin TX

A dual-core baseband processor IC for GSM/GPRS cellular phone applications is built in a 0.13 μ m CMOS process with 5 levels of copper interconnect and contains a high level of mixed-signal integration which includes: 1GHz CMOS synthesizer, 10b general-purpose ADC, two 14b ADCs, power amplifier controller, and 13b voice CODEC.

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Z. Zheng

3.7 A $0.55\text{nV}/\sqrt{\text{Hz}}$ Gigabit Fully-Differential CMOS Preamplifier for MR/GMR Read Application

Zhiliang Zheng, Steven Lam, Sehat Sutardja

Marvell Semiconductor, Inc., Sunnyvale, CA

A low-noise Gb fully differential preamp in $0.25\mu\text{m}$ CMOS has a variable gain with constant 850MHz bandwidth, and has a variable bandwidth with constant gain. Noise is $<0.55\text{nV}/\sqrt{\text{Hz}}$. The power consumption is 600mW. The die of a 4-channel IC is $<4.2\text{mm}^2$.

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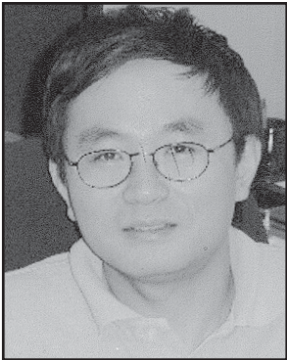


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F. Yang

4.1 A 1.5V 86mW/ch 8-Channel 622-3125Mb/s/ch CMOS SerDes Macrocell with Selectable MUX/DEMUX Ratio

Fuji Yang, Jay O'Neill, Patrik Larsson, Dave Inglis, Joe Othmer

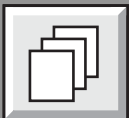
Agere Systems, Holmdel, NJ

An 8-channel serial link transceiver realizes 20Gb/s full duplex total I/O throughput with <700mW dissipation from a 1.5V supply and occupies 2mm² in 0.16μm CMOS. An analog DLL allows tracking of frequency offset up to 400ppm. The receiver, employing an integrate-and-dump front-end, achieves 30mVpp sensitivity.

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D. Zheng

4.2 A Quad 3.125Gbps/Channel Transceiver with Analog Phase Rotators

Dong Zheng, Xuecheng Jin, Eugene Cheung, Manoj Rana, Ge Song, Yong Jiang, Yue-Hong Sutu, Bin Wu

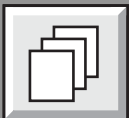
BitBlitz Communications, Fremont, CA

A $0.18\mu\text{m}^2$ CMOS quad transceiver provides 12.5Gb/s full-duplex raw data throughput at 200mW/channel consumption. An analog phase rotator in CDR eliminates quantization error of digital phase interpolation techniques, resulting in $<17\text{ps}$ peak-peak output jitter.

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P. Landman

4.3 A 62Gb/s Backplane Interconnect ASIC Based on 3.1Gb/s Serial-Link Technology

Paul Landman, Ah-Lyan Yee, Richard Gu, Bharadwaj Parthasarathy, Vikas Gupta, Sridhar Ramaswamy, Lisa Dyson, Pat Bosshart, Jeffrey Reynolds, Mats Frännhagen¹, Per Fremrot¹, Stefan Johansson¹, Keith Lewis¹, Wai Lee

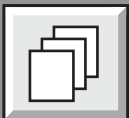
Texas Instruments, Dallas, TX, ¹Turin Networks, Petaluma, CA

A backplane interconnect ASIC with 62Gb/s full-duplex aggregate throughput uses 3.1Gb/s serial link technology organized as 20 bidirectional channels to realize bandwidth. The chip operates with $<5 \times 10^{-17}$ aggregate BER and is fabricated in a 0.18 μm CMOS technology, dissipating 9W in a 768-pin flipchip BGA package.

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T. Ebuchi

4.4 An 800Mb/s Physical Layer LSI with Hybrid Port Architecture for Consumer Electronics Networking

Takefumi Yoshikawk, Tadahiro Yoshida, Tsuyoshi Ebuchi, Yukio Arima, Toru Iwata, Kazuko Nishimura, Hiroshi Kimura, Yoshihide Komatsu, Hiroyuki Yamauchi

Matsushita Electric Industrial Co., Ltd., Osaka, Japan

A physical layer LSI has one DS-port and two β ports in accordance with IEEE1394-2000 and P1394b Draft 1.01 respectively. The 0.25 μ m CMOS LSI realizes 800Mb/s and 1.2km peer-to-peer IEEE1394 networking through β port. Each β port requires 180mW active power and is treated as ASIC macro for future large system integration.

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R. Farjad-rad

4.5 A 0.2-2GHz 12mW Multiplying DLL for Low-Jitter Clock Synthesis in Highly-Integrated Data-Communication Chips

Ramin Farjad-rad, William Dally, Hoik-Tiaq Ng, John Poulton, Teva Stone, Rohit Rathi, Edward Lee, David Huang, John Edmondson, Ramesh Senthinathan

Velio Communications Inc., Milpitas, CA

The MDLL, in 0.18 μ m CMOS, has 0.05mm² active area and 200MHz to 2GHz speed range. The complete synthesizer, including the output clock buffers, dissipates 12mW from a 1.8V supply at 2.0GHz. This MDLL architecture is used as a clock multiplier in a highly-integrated chip, and has jitter of 1.73ps (rms) and 15.6ps (pk-pk) at 2GHz.

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S. Ye

4.6 A Multiple-Crystal Interface PLL with VCO Realignment to Reduce Phase Noise

Sheng Ye^{1,3}, Lars Jansson², Ian Galton¹

¹University of California at San Diego, La Jolla, CA, ²Silicon Wave Corporation, San Diego, CA, ³Now with Silicon Wave Corporation, San Diego, CA

A phase realignment technique is applied to a ring oscillator VCO in a 3V 6.8mW CMOS PLL that converts most of the popular crystal reference frequencies to a 32MHz baseband clock and RF PLL reference. The peak in-band phase noise at 20kHz offset is -102dBc/Hz with the technique enabled, and -92dBc/Hz with the technique disabled.

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J. Lee

4.7 A Multichip on Oxide 1Gb/s 80dB Fully-Differential CMOS Transimpedance Amplifier for Optical Interconnect Applications

Jaeseo Lee, Seong-Jun Song, Sung Min Park, Choong-Mo Nam¹,
Young-Se Kwon, Hoi-Jun Yoo

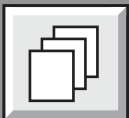
Dept. of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Taejeon, Korea, ¹Telephus, Taejeon, Korea

A 1.0Gb/s 80dB Ω fully-differential TIA uses 0.25 μ m CMOS and multichip-on-oxide (MCO) process. MCO enables integration of PD, TIA, and planar inductors of Q=21.1 for shunt peaking on an oxidized silicon substrate. Interchannel crosstalk and power dissipation are <-40dB and 27mW, respectively. MCO and TIA chips are 5x5mm² and 0.7x1mm², respectively.

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S. Hackl

4.8 A 45GHz SiGe Active Frequency Multiplier

**Sabine Hackl^{1,2}, Josef Böck¹, Günter Ritzberger^{1,2}, Martin Wurzer¹,
Herbert Knapp¹, Ludwig Treitinger¹, Arpad L. Scholtz²**

¹Infineon Technologies AG, Munich, Germany

²Technical University of Vienna, Austria

A frequency quadrupler for frequencies up to 45GHz uses a pre-production 0.4 μ m SiGe bipolar technology. Gain is achieved at -15dBm input power between 24 and 45GHz with maximum of 7.3dB at 44GHz. The circuit draws 84mA from a single 5V supply.

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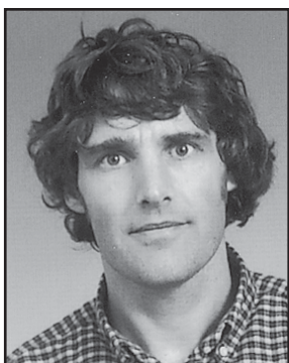


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P. van Zeijl

5.1 A Bluetooth Radio in 0.18 μ m CMOS

Paul T.M. van Zeijl, Jan-Wim Eikenbroek, Peter-Paul Vervoort, Suma Setty¹, Jurjen Tangenberg, Gary Shipton¹, Eric Kooistra, Ids Keekstra, Didier Belot²

Ericsson Eurolab Netherlands, Emmen, the Netherlands, ¹Ericsson Microelectronics, Swindon, UK, ²STMicroelectronics, Crolles, France

A Bluetooth radio in 0.18 μ m CMOS technology works on 2.5-3.0V, dissipating 75mW in RX and 90mW in TX. RX uses a 2MHz IF with an active poly-phase bandpass filter. The fractional-N PLL uses a VCO running at 5GHz. TX uses IQ modulation. Special attention is paid to Si-crosstalk because this radio is combined with baseband circuitry. Silicon area is 5.5mm².

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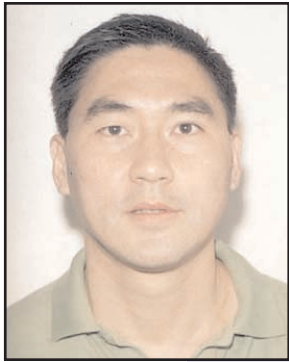


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G. Chang

5.2 A Direct-Conversion Single-Chip Radio-Modem for Bluetooth

Glenn Chang, Lars Jansson, Kevin Wang, Jorge Grilo, Raymond Montemayor, Chris Hull¹, Mark Lane, A. X. Estrada, Mike Anderson, Ian Galton, S. V. Kishore

Silicon Wave Corporation, San Diego, CA

¹Now with National Semiconductor, San Diego, CA

A fully-integrated radio-modem using a direct-conversion receiver architecture achieves -83dBm sensitivity at 0.1% BER, +40dBm IIP2, and -5dB and -40dB adjacent and alternate channel blocking C/I, respectively. The radio consumes 39mA in receive and 37mA in transmit mode with a 2.7V supply. The 19.5mm² chip uses a 0.35 μ m 27GHz f_T SOI BiCMOS process.

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J. Cheah

5.3 Design of a Low-Cost Integrated 0.25 μ m CMOS Bluetooth SOC in 16.5mm² Silicon Area

Jonathon Cheah, Ee-Hong Kwek, Eng Chuan Low, Chee Kwang Quek,
Christopher Yong, Roy Enright, Jacob Hirbawi, Andrew Lee,
Hongyu Xie, Longyin Wei, Le Luong, Jianping Pan,
Shih-Tsung Yang, Wing Fat Andy Lau, Wai-Lim Ngai

Transilica Inc., San Diego, CA

A complete 0.25 μ m CMOS SOC Bluetooth solution adopts a two-die in a single MCM chip packaging approach with minimum product cost as the most important design goal while maintaining competitive power consumption and RF performance.

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D. Su

5.4 A 5GHz CMOS Transceiver for IEEE 802.11a Wireless LAN

**David Su, Masoud Zargari, Patrick Yue, Shahriar Rabii,
David Weber, Brian Kaczynski, Srenik Mehta, Kalwant Singh,
Sunetra Mendis, Bruce Wooley¹**

Atheros Communications, Sunnyvale, California

¹Stanford University, Stanford, California

A 5GHz transceiver comprising the RF and analog circuits of an IEEE 802.11a-complaint WLAN using a 0.25 μ m CMOS technology occupies 22mm². The IC has 22dBm maximum transmitted power, 8dB overall receive-chain noise figure, and -112dBc/Hz synthesizer phase noise at 1MHz offset.

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M. Kokubo

5.5 A 2.4GHz RF Transceiver with Digital Channel-Selection Filter for Bluetooth

Masaru Kokubo, Masaaki Shida, Takashi Ishikawa, Hiroki Sonoda, Katsumi Yamamoto, Tatsuji Matsuura, Masaharu Matsuoka, Takefumi Endo, Takao Kobayashi, Katsumi Oosaki, Takaaki Henmi, Junya Kudoh, Hirokazu Miyagawa

Hitachi Ltd., Tokyo, Japan

An RF transceiver chip for Bluetooth that uses a digital channel-selection filter is $3.3 \times 3.4 \text{mm}^2$, realized by decrease of the analog area using the digital channel selection filter. The test chip uses $0.35 \mu\text{m}$ BiCMOS.

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T. Masuda

5.6 Single-Chip 5.8GHz ETC Transceiver IC with PLL and Demodulation Circuits using SiGe HBT/CMOS

Toru Masuda, Ken-ichi Ohhata¹, Nobuhiro Shiramizu, Satoshi Hanazawa², Masaki Kudoh³, Yuko Tanba², Yusuke Takeuchi², Hiromi Shimamoto¹, Toshio Nagashima⁴, Katsuyoshi Washio

Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo, Japan, ¹Musashino Office, Hitachi Device Engineering, Co. Ltd., Kokubunji, Tokyo, Japan, ²Device Development Center, Hitachi, Ltd., Ome, Tokyo, Japan, ³Hitachi ULSI Systems Co., Ltd., Ome, Tokyo, Japan, ⁴Digital Media Systems, R&D Division, Hitachi, Ltd., Totsuka, Kanagawa, Japan

A single-chip 5.8GHz ETC transceiver IC with PLL and demodulator uses SiGe HBT/CMOS. The fully integrated ETC chip includes a 31dB-gain RX stage, an ASK demodulator, and a high-precision RSSI. The PLL is constructed with a varactor-tuned LC-VCO and a low-power BiCMOS synthesizer. The TX stage incorporates a transformer-transferred single-ended PA.

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E. Maayan

6.1 A 512Mb NROM Flash Data Storage Memory with 8MB/s Data Rate

Eduardo Maayan¹, Ran Dvir¹, Joseph Shor¹, Yan Polansky¹, Yair Sofer¹, Ilan Bloom¹, Dror Avni¹, Boaz Eitan¹, Zeev Cohen², Moshe Meyassed², Yair Alpern², Herbert Palm³, Elard Stein v. Kamienski⁴, Patrick Haibach⁴, Dirk Caspary⁴, Stephan Riedel⁴, Roman Knöfler⁴

¹Saifun Semiconductors Ltd., Netanya, Israel, ²Ingentix Ltd., Netanya, Israel,

³Ingentix GmbH, Düsseldorf, Germany, ⁴Infineon Technologies, Dresden, Germany

The NROM technology is applied to EEPROM, Flash, and data storage product lines. All the products are based on the two-bit-per-cell core technology, using common design concepts, algorithms, circuits, and the same process architecture. Differing product requirements emphasize versatility of the concept.

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T. Tanzawa

6.2 A 44mm² 4-Bank 8-Word Page Read 64Mb Flash Memory with Flexible Block Redundancy and Fast Accurate Word-Line Voltage Controller

T. Tanzawa, A. Umezawa, T. Taura, H. Shiga, T. Hara, Y. Takano, T. Miyaba¹, N. Tokiwa¹, K. Watanabe, H. Watanabe, K. Masuda, K. Naruke, H. Kato, S. Atsumi

Toshiba Corporation, Yokohama, Japan, ¹Toshiba Microelectronics Corporation, Yokohama, Japan

Combining a negative-gate channel-erasing NOR flash memory technology with an aggressively-scaled NAND Flash process technology results in a 64Mb NOR flash memory with 0.27 μ m² cell and 44mm² chip. The Flash memory provides 4 independent banks for flexible dual operation and unique block redundancy for yield.

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J. Lee

6.3 A 1.8V 1Gb NAND Flash Memory with 0.12 μ m STI Process Technology

June Lee, Heung-Soo Im, Dae-Seok Byeon, Kyeong-Han Lee, Dong-Hyuk Chae, Kyong-Hwa Lee, Young-Ho Lim, Jung-Dal Choi, Young-Il Seo, Jong-Sik Lee, Kang-Deog Suh

Samsung Electronics, Kyunggi, Korea

A 1.8V 1Gb Flash memory uses a 0.12 μ m STI process technology. A charge pump operates at <1.8V. A center-placed row decoder is digitized in one block pitch by applying 32-cell NAND structure. A page buffer, containing two latches, supports cache-program to improve program speed to 7MB/s.

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K. Takeuchi

6.4 A 125mm² 1Gb NAND Flash Memory with 10MB/s Program Throughput

Hiroshi Nakamura, Kenichi Imamiya, Toshihiko Himeno, Toshio Yamamura, Tamio Ikehashi, Ken Takeuchi, Kazushige Kanda, Koji Hosono, Takuya Futatsuyama, Koichi Kawai, Riichiro Shirota, Norihisa Arai, Fumitaka Arai, Kazuo Hatakeyama, Hiroaki Hazama, Masanobu Saito, Hisataka Meguro, Kevin Conley¹, Khandker Quader¹, Jian Chen¹

Toshiba Corporation, Yokohama, Kanagawa, Japan

¹Sandisk Corporation, Sunnyvale, CA

A 125mm² 1Gb NAND flash uses 0.13 μ m CMOS. The cell is 0.077 μ m². Chip architecture is changed to reduce chip size and to realize 10.6MB/s throughput for program and 20MB/s for read. An on-chip page copy function provides 9.4MB/s throughput for garbage collection.

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B-D. Yang

6.5 A Low-Power ROM using Charge Recycling and Charge Sharing

Byung-Do Yang, Lee-Sup Kim

Department of EECS, KAIST, Yuseong-Gu, Daejeon, Korea

A charge-recycling predecoder (CRPD), a charge-recycling word line decoder (CRWD), and a charge-sharing bit line (CSBL) reduce power in a memory. The CRPD and the CRWD recycle the charge used in predecoder lines and word lines. The CSBL reduces the bit line swing voltage. A 128kb ROM in a 0.35 μ m CMOS process consumes 8.63mW at 100MHz and 3.3V.

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D. E. Bradley

6.6 The 16kB Single-Cycle Read Access Cache on a Next-Generation 64b Itanium Microprocessor

David Bradley, Patrick Mahoney¹, Blaine Stackhouse

Hewlett-Packard Co., ¹Intel Corp., Fort Collins, CO

A 16kB four-ported physically addressed cache operates at 1.2GHz with 19.2GB/s peak bandwidth. Circuit and microarchitectural techniques are optimized to allow a single-cycle read access latency. The cache occupies 3.2x1.8mm² in a 0.18μm process.

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J. Wu

6.7 An On-Chip 3MB Subarray-Based 3rd Level Cache on an Itanium Microprocessor

Don Weiss, John J. Wu, Victor Chin¹

Hewlett-Packard Company, Fort Collins, CO, ¹Intel Corp., Santa Clara, CA

This 3MB on-chip level-three cache employs subarray design style, and achieves 85% array efficiency. Characterized to operate up to 1.2GHz, the cache allows a store and a load in every four core cycles, and provides a total bandwidth of 64GB/s at 1.0GHz.

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C. Thomas

7.1 A Unified Turbo / Viterbi Channel Decoder for 3GPP Mobile Wireless in 0.18 μ m CMOS

Mark Bickerstaff¹, David Garrett¹, Thomas Prokop², Charles Thomas², Benjamin Widdup², Gongyu Zhou², Chris Nicol², Ran-Hong Yan¹

¹Bell Labs Research, ²Wireless Networks Group, Bell Labs, Lucent Technologies, North Ryde, Australia

A 3GPP-compliant 4.1Mb/s channel decoder supports data and voice calls in a unified Turbo/Viterbi architecture with hardware interleaver memory and pattern computation. The 9mm² chip in 0.18 μ m 1.8V 6LM CMOS operates at 110MHz and consumes 306mW when decoding 2Mb/s data and voice calls.

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J. S. Thomson

7.2 An Integrated 802.11a Baseband and MAC Processor

John Thomson, Bevan Baas, Elizabeth M. Cooper, Jeffrey M. Gilbert, George Hsieh, Paul Husted, Aparna Lokanathan, Jeffrey S. Kuskin, David McCracken, Bill McFarland, Teresa H. Meng, David Nakahira, Samuel Ng, Mahesh Rattehalli, Jeff L. Smith, Ravi Subramanian, Lars Thon, Yi-Hsiu Wang, Robert Yu, Xiaoru Zhang

Atheros Communications, Sunnyvale, CA

An 0.25 μ m CMOS mixed-signal baseband and MAC processor for the IEEE 802.11a WLAN standard in 0.25 μ m CMOS occupies 6.8x6.8mm² and contains 4.0M transistors in a 196-pin BGA package. Power consumption for transmit and receive is 326mW and 452mW. Additional data rates up to 108Mb/s are supported.

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L. Song

7.3 A 10Gb/s and 40Gb/s Forward-Error-Correction Device for Optical Communications

Leilei Song, Meng-Lin Yu, Michael S. Shaffer

High-Speed Communications VLSI Research, Agere Systems, Holmdel, NJ

Two forward error-correcting devices for OC-48/192/768 are implemented in 1.5V 0.6 μ m CMOS. A 10Gb/s (or Quad 2.5Gb/s) device with 424k-gate Reed-Solomon core consumes 343mW. A 40Gb/s device contains 364k-gates and consumes 361mW.

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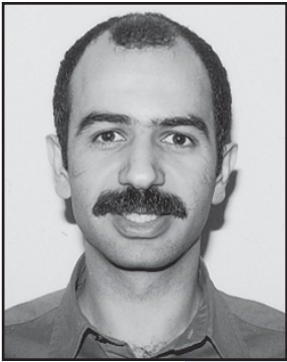


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S. Mirabbasi

7.4 IIR Digital Filter for $\Delta\Sigma$ Decimation, Channel Selection, and Square-Root Raised-Cosine Nyquist Filtering

Shahriar Mirabbasi, Ken Martin

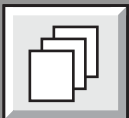
Department of Electrical and Computer Engineering, University of Toronto, Toronto,
Ontario, Canada

A 1.8V 0.18 μ m CMOS $\Delta\Sigma$ decimation filter also performs channel-selection and an approximate root-raised-cosine Nyquist pulse-shaping. The 0.1mm² IIR structure consumes 6.4mW (26.8mW) at 64MHz (240MHz) oversampling frequency.

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A. Torosyan

7.5 A 300MHz Quadrature Direct Digital Synthesizer/Mixer in 0.25 μ m CMOS

Arthur Torosyan, Dengwei Fu, Alan N. Willson, Jr.

Electrical Engineering Department, University of California, Los Angeles, CA

A 0.25 μ m quadrature direct digital frequency synthesizer/mixer has 32b frequency control word, 0.07Hz tuning resolution, 12b inputs and 13b outputs offering 90.3dBc spurious-free dynamic range. The 4180 cell core occupies 0.36mm². Power dissipation is <400mW at 300MHz.

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D. De Caro

7.6 Direct Digital Frequency Synthesizers using High-Order Polynomial Approximation

D. De Caro, E. Napoli, A.G.M. Strollo

University of Naples "Federico II" – Dept. of Electronic Engineering

Two 80MHz 0.35 μ m 3.3V CMOS ROM-less DDFS using polynomial approximation are compared with Cordic-based circuits. A 60dBc SFDR DDFS uses 2nd-order polynomials and 0.18mm², with 15mW dissipation. An 80dBc SFDR DDFS uses 3rd-order polynomials and 0.44mm², with 35mW dissipation.

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M. Mansuri

8.1 Jitter Optimization Based on Phase-Locked Loop Design Parameters

Mozhgan Mansuri, Chih-Kong Ken Yang

University of California, Los Angeles, CA

A tunable PLL allows independent optimization of loop parameters. The effects of varying PLL parameters (damping factor and bandwidth) on timing jitter is derived analytically and verified experimentally.

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I. Hwang

8.2 A Self-Regulating VCO with Supply Sensitivity of $<0.15\%$ -Delay/ 1% -Supply

In-Chul Hwang¹, Sung-Mo (Steve) Kang²

¹Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, IL

²Baskin School of Engineering, University of California, Santa Cruz, CA

A self-regulating VCO has supply sensitivity $<0.15\%$ -delay/ 1% -supply. The design uses a differential delay cell that contains an nMOS transmission gate for delay adjustment and a built-in feedback circuit for power-supply rejection. The charge-pump PLL embedded with this VCO has 40ps peak-to-peak jitter at 450MHz output with VCO at 900MHz.

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C. Kim

8.3 Low-Power Small-Area ± 7.28 ps Jitter 1GHz DLL-Based Clock Generator

Chulwoo Kim¹, In-Chul Hwang², Sung-Mo Kang³

^{1,2}University of Illinois, Urbana, IL, ¹now with IBM Microelectronics Division, Austin, TX,

³University of California, Santa Cruz, CA

A 1GHz DLL-based clock generator in 0.35 μ m CMOS occupies 0.08mm². It has fast locking time and no jitter-accumulation problem. A phase detector with reset circuitry and a frequency multiplier overcome the limited locking range and frequency multiplication problem of conventional DLL-based systems. Measured peak-to-peak jitter is ± 7.28 ps.

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P. Restle

8.4 The Clock Distribution of the POWER4 Microprocessor

**Phillip J. Restle, Craig A. Carter², James P. Eckhardt³,
Byron L. Krauter², Bradley D. McCredie², Keith A. Jenkins,
Alan J. Weger, Anthony V. Mule⁴**

IBM Research, Yorktown Heights, NY, ²IBM Enterprise Systems Group, Austin, TX,
³IBM Enterprise Systems Group, Poughkeepsie, NY, ⁴Georgia Institute of
Technology, Atlanta, GA

The clock distribution on the Power4 supplies a single critical 1.5GHz clock from one SOI-optimized PLL to 15,200 pins on a large chip with 20ps skew and 35ps jitter. The network contains 64 tuned trees driving a single grid, and specialized tools to achieve targets on schedule with no adjustment circuitry.

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F. Anderson

8.5 The Core Clock System on the Next-Generation Itanium™ Microprocessor

Ferd E. Anderson, J. Steve Wells¹, Eugene Z. Berta²

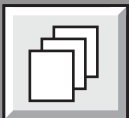
Intel Corp., ¹Hewlett Packard Corp., ²Hewlett Packard Corp., Fort Collins, CO

A PLL generates a high-frequency core clock for a 1GHz processor by multiplying up the system clock. The clock is distributed across the 19x14mm² core via a shielded, balanced, H-tree to the final pulsed gated buffers with <62ps measured skew. Test features include phase shrinking and regional skew manipulation.

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S. Geissler

8.6 A Low-Power RISC Microprocessor using Dual PLLs in a 0.13 μ m SOI Technology with Copper Interconnect and Low-k BEOL Dielectric

Stephen Geissler, David Appenzeller, Erwin Cohen, Steven Charlebois, Paul Kartschoke, Peter McCormick, Norman Rohrer, Gerard Salem, Peter Sandon, Bruce Singer, Timothy Von Reyn, Jeffrey Zimmerman

IBM Microelectronics Division, Essex Junction, VT

Microprocessors achieving clock frequencies >1GHz for mobile applications require solutions to maintain long battery life. Circuit and architecture solutions for dynamic frequency switching between multiple PLLs, DC power reduction methods, and impact of low-k dielectric on timing and power are discussed.

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T. Ohsawa

9.1 Memory Design Using One-Transistor Gain Cell on SOI

**Takashi Ohsawa, Katsuyuki Fujita, Tomoki Higashi¹, Yoshihisa Iwata,
Takeshi Kajiyama, Yoshiaki Asao, Kazumasa Sunouchi**

Memory LSI Research and Development Center, Memory Division, Toshiba Corporation Semiconductor Company, Yokohama, Japan, ¹Memory Device Engineering Department, Toshiba Microelectronics Corporation, Yokohama, Japan

A 512kb DRAM has a $7F^2$ one-transistor gain cell ($F=0.18\mu\text{m}$) on SOI. The array driving method makes selective write possible. Basic operation is verified by device simulation and hardware measurement. Simulations show 40ns access time. Non-destructive readout and Cb/Cs-free signal development improve cell efficiency.

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S. Hong

9.2 An Offset Cancellation Bit-Line Sensing Scheme for Low-Voltage DRAM Applications

Sang Hoon Hong, Si Hong Kim, Se Jun Kim, Jae-Kyung Wee, Jin Yong Chung

Hynix Semiconductor Inc., Ichon, Kyoung-gi, Korea

Offset-cancellation provides low-voltage DRAM operation. The offset cancelling bit-line sense amplifiers are pitch-matched to the conventional 0.16 μ m DRAM cell array without process modifications. Results indicate better refresh characteristics than conventional bit-line sense amplifiers even at 1.5V.

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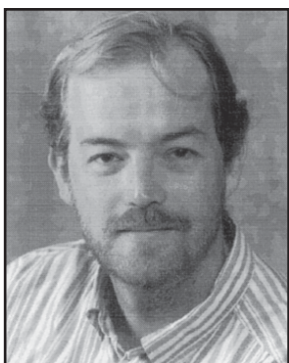


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J. Barth

9.3 A 300MHz Multi-Banked, eDRAM Macro Featuring GND Sense, Bit-Line Twisting and Direct Reference Cell Write

John Barth, Darren Anand, Jeff Dreibelbis, Erik Nelson

IBM MicroElectronics, Burlington, VT

A 0.12 μ m growable eDRAM macro has GND sense, bit-line twisting, direct reference cell write, a flexible multi-banking protocol, and column redundancy to support multi-banking. The protocol supports simultaneous activate, read/write and pre-charge to three different banks. Hardware measurements verify 300MHz operation, 6.6ns tacc, and 10ns trc.

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H-B. Kang

9.4 A Hierarchy Bitline Boost Scheme for Sub-1.5V Operation and Short Precharge Time on High Density FeRAM

Hee-Bok Kang, Hun-Woo Kye, Geun-Il Lee, Je-Hoon Park, Jung-Hwan Kim, Seaung-Suk Lee, Suk-Kyoung Hong, Young-Jin Park, Jin-Yong Chung

Memory R&D Center, Hynix Semiconductor, Ichon, Kyunggi, Republic of Korea

This work develops three concepts: low-voltage operation with boost voltage control of bitline and plateline, reduced bitline capacitance with multiple divided sub cell array, and increased chip performance with write operation sharing both active and precharge time period. A 256kb test chip with $3.0 \times 1.0 \mu\text{m}^2$ 1T1C memory cells in $0.25 \mu\text{m}$ design rules is expected to achieve 180ns access and 70ns precharge at 1.5V based on internal probing.

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T. Nishihara

9.5 A Quasi-Matrix Ferroelectric Memory for Future Silicon Storage

Toshiyuki Nishihara, Yasuyuki Ito

Sony Corporation, Tokyo, Japan

A memory unit consists of multiple ferroelectric capacitors that store individual bits and share one access transistor. Disturb degradation and cross-talk effects are suppressed to an acceptable level. The capacitors can be multi-stacked, increasing packing density by a number of times.

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B-G Jeon

9.6 A 0.25 μ m 3.0V 1T1C 32Mb Nonvolatile Ferroelectric RAM with Address Transition Detector (ATD) and Current Forcing Latch Sense Amplifier (CFLSA) Scheme

Mun-Kyu Choi, Byung-Gil Jeon, Nakwon Jang, Byung-Jun Min,
Yoon-Jong Song, Sung-Yung Lee, Hyun-Ho Kim, Dong-Jin Jung,
Heung-Jin Joo, Kinam Kim

Samsung Electronics, Kiheung, Korea

A nonvolatile 32Mb ferroelectric random-access memory with 0.25 μ m design rules uses ATD control for SRAM applications and a common-plate folded bit-line cell scheme with current forcing latched sense amp for low noise level without cell area penalty.

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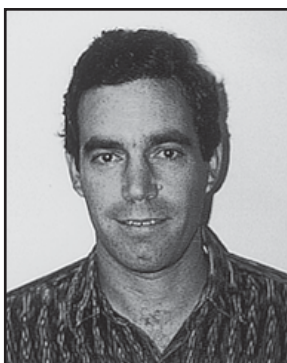


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R. Neff

10.1 A 4GSample/s 8b ADC in 0.35 μ m CMOS

**Ken Poulton, Robert Neff, Art Muto, Wei Liu¹, Andy Burstein²,
Mehrdad Heshami³**

Agilent Technologies, Palo Alto, CA, ¹Colorado Springs, CO, ²now with Volterra
Semiconductor, Fremont, CA, ³now with Virata, Cupertino, CA

A 4GSample/s 8b ADC in 0.35 μ m CMOS achieves accuracy of 7 effective bits at DC and 6.1 effective bits for 1GHz input, while dissipating 4.6W. It uses 32 current-mode pipelines driven by 32 interleaved clocks with 1.1ps rms accuracy.

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P. Scholtens

10.2 A 6b 1.6GSample/s Flash ADC in 0.18 μ m CMOS Using Averaging Termination

Peter Scholtens, Maarten Vertregt

Philips Research Laboratories, Eindhoven, the Netherlands

A 1.6GSample/s 6b flash analog-to-digital converter in 0.18 μ m CMOS is for storage read channels. The array of amplifiers and averaging resistors is terminated with less overrange while maintaining full-scale linearity. Consuming 340mW, it achieves 5.7 effective bits at DC and 5 effective bits at 660MHz.

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K. Sushihara

10.3 A 7b 450MSample/s 50mW CMOS ADC in 0.3mm²

Koji Sushihara, Akira Matsuzawa

Matsushita Electric Industrial Co., Ltd., Osaka, Japan

A 7b 450MSample/s CMOS ADC in 0.18 μ m technology is used for the embedded digital read channel system in DVD SOC. A dynamic comparator and an interpolation circuit composed of gate-width-weighted transistors consumes 50mW and occupies 0.3mm².

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S. Jamal

10.4 A 10b 120MSample/s Time-Interleaved Analog-to-Digital Converter with Digital Background Calibration

Shafiq M. Jamal¹, Daihong Fu², Paul J. Hurst, Stephen H. Lewis

Dept. of Electrical and Computer Engineering, University of California, Davis, CA

¹Now with Marvell Semiconductor, Sunnyvale, CA

²Now with Maxim Integrated Products, Sunnyvale, CA

Digital calibration using adaptive signal processing corrects offset mismatch, gain mismatch, and sample-time error between time-interleaved channels in a 10b 120MSample/s pipelined ADC. With background calibration, peak SNDR is 56.8dB and power dissipation is 234mW from 3.3V. Active area is 12.5mm² in 0.35μm CMOS.

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D. Miyazaki

10.5 A 16mW 30MSample/s 10b Pipelined A/D Converter using a Pseudo-Differential Architecture

Daisuke Miyazaki, Masanori Furuta, Shoji Kawahito¹

Graduate School of Electronics Science and Technology, ¹Research Institute of Electronics, Shizuoka University, Hamamatsu, Japan

A 16mW 2V 30MSample/s 10b pipelined A/D converter in 0.3 μ m CMOS uses a pseudo-differential architecture and a capacitor cross-coupled S/H stage. SNDR and the SFDR at 30MHz input are 54dB and 67dB, respectively.

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F. Kuttner

10.6 A 1.2V 10b 20MSample/s Non-Binary Successive Approximation ADC in 0.13 μ m CMOS

Franz Kuttner

Infineon Technologies AG, Microelectronics Design Centers Austria, Villach, Austria

A successive-approximation ADC with non-binary code achieves 55dB SNR at sampling frequencies up to 20MHz. The converter, with on-chip driver for analog input and reference input, measures 0.08mm² in a standard 0.13 μ m CMOS process and consumes 12mW from a single 1.2V supply.

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A. Joseph

11.1 0.13 μ m 210GHz f_T SiGe HBTs - Expanding the Horizons of SiGe BiCMOS

A. Joseph, D. Coolbaugh, D. Harambe, G. Freeman¹, S. Subbanna¹, M. Doherty³, J. Dunn, C. Dickey, D. Greenberg², R. Groves¹, M. Meghelli², A. Rylyakov², M. Sorna¹, O. Schreiber⁴, D. Herman², T. Tanji⁵

IBM, Essex Jct., VT / ¹Hopewell Junction, NY / ²Yorktown Heights, NY / ³Lowell, MA, / ⁴AMCC, San Diego, CA / ⁵Edina, MN

SiGe BiCMOS is in its fourth lithographic generation since introduction of the 0.5 μ m. The key component is the SiGe-base HBT whose performance (f_T , f_{MAX}) is improved to >200GHz in the 0.13 μ m generation. Evolution and future directions of SiGe BiCMOS technology and product applications are reviewed.

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M. Takamiya

11.2 An On-Chip 100GHz-Sampling 8-channel Sampling Oscilloscope with Embedded Sampling Clock Generator

Makoto Takamiya, Masayuki Mizuno, ¹Kazuyuki Nakamura

NEC Corp., Kanagawa, Japan, ¹now with Kyushu Institute of Technology, Fukuoka,
Japan

An on-chip 8-channel sampling oscilloscope macro for signal integrity checking uses a 0.13 μ m CMOS process. It contains a phase-interpolated sampling clock generator for 100GHz sampling, charge-sharing sampling heads with -0.3V to V_{dd}+0.3V input range, and ESD-tolerant decoupling capacitors for noise-immune measurement.

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R. C. Ruby

11.3 High-Q FBAR Filters in a Wafer-Level Chip-Scale Package

R. C. Ruby, A. Barfknecht, C. Han, Y. Desai, F. Geefay, G. Gan, M. Gat, T. Verhoeven

Agilent, Newark, CA

Wafer-level chip-scale packaged RF filters use thin-film bulk acoustic resonator technology. The $1 \times 1 \text{ mm}^2$ high-Q filter is hermetically sealed as two thin layers of silicon for $\sim 12 \text{ mil}$ height. The full-band 1900MHz Tx filter mounted in a PCS power module has a 12MHz roll-off, and replaces external split-band SAW filters and their accompanying switches

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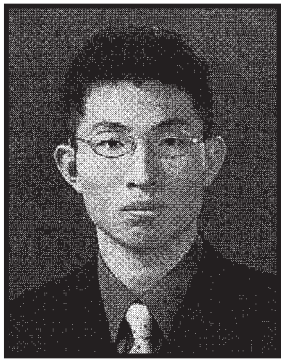


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Y. Ku

11.4 Polylithic Integration of a SAW Quartz-on-Silicon Oscillator for Single-Chip Radio

Yeonwoo Ku, Yunseong Eo¹, Kwyro Lee

Dept. EECS and MICROS Research Center, KAIST, Taejon, Republic of Korea

¹LG Electronics Institute of Technology, Republic of Korea

A digitally temperature-compensated SAW oscillator uses Polylithic IC technology on a quartz-on-silicon wafer. The oscillator shows -115dBc/Hz phase noise at 10kHz offset, 7.5mW power consumption, and 4.5ppm frequency stability.

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J. F. Bulzacchelli

11.5 Superconducting Bandpass $\Delta\Sigma$ Modulator with 2.23GHz Center Frequency and 42.6GHz Sampling Rate

John F. Bulzacchelli, Hae-Seung Lee, James A. Misewich¹, Mark B. Ketchen¹

Massachusetts Institute of Technology, Cambridge, MA

¹IBM T.J. Watson Research Center, Yorktown Heights, NY

A superconducting bandpass $\Delta\Sigma$ modulator employing a 2.23GHz microstrip resonator and a single flux quantum comparator clocked at 42.6GHz achieves 49dB peak SNR over a 20.8MHz bandwidth. At 40.2GHz clock rate, in-band noise over a 19.6MHz bandwidth is -57dBFS. The test chip with integrated acquisition memory contains 4065 Josephson junctions and dissipates 1.9mW at T=4.2K.

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Y. Nakasha

11.6 A 43Gb/s Full-Rate-Clock 4:1 Multiplexer in InP-based HEMT Technology

Yasuhiro Nakasha, Toshihide Suzuki, Hideki Kano, Akio Ohya¹, Ken Sawada, Kozo Makiyama, Tsuyoshi Takahashi, Masahiro Nishi¹, Tatsuya Hirose, Masahiko Takikawa, Yuu Watanabe

Fujitsu Laboratories, Ltd., Atsugi, Japan

¹Fujitsu Quantum Devices Ltd., Yamanashi, Japan

A 43Gb/s 4:1 multiplexer in 0.13 μ m InP-based HEMT technology contains a 52Gb/s static D-FF and a phase adjuster giving the D-FF 360 $^{\circ}$ effective phase margin. Microwave techniques and optimization of layout enable 43Gb/s operation with 43GHz full-rate clock. Power dissipation is 7.9W at -5.2V.

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T. Suzuki

11.7 A 90Gb/s 2:1 Multiplexer IC in InP-based HEMT Technology

**Toshihide Suzuki, Yasuhiro Nakasha, Tsuyoshi Takahashi,
Kouzou Makiyama, Kenji Imanishi, Tatsuya Hirose, Yuu Watanabe**

Fujitsu Laboratories Ltd., Atsugi, Kanagawa, Japan

A 90Gb/s 2:1 multiplexer IC uses 0.13 μ m-gate InP-based HEMT technology. Parallel 2-ch input data are serialized. The differential outputs are 0.7V_{pp}. The 1.9x1.8mm² die consumes 1.3W from a -5.2V supply.

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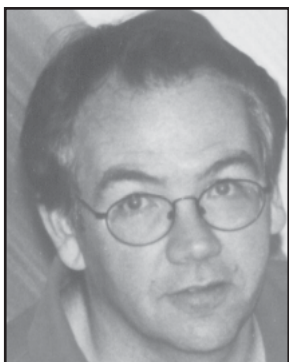


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A. Gara

12.1 Cellular Supercomputing with System-On-A-Chip

G. Almasi, G. S. Almasi, D. Beece, R. Bellofatto, G. Bhanot, R. Bickford, M. Blumrich, A. A. Bright, J. Brunheroto, C. Cascaval, J. Castaños, L. Ceze, P. Coteus, S. Chatterjee, D. Chen, G. Chiu, T. M. Cipolla, P. Crumley, A. Deutsch, M. B. Dombrowa, W. Donath, M. Eleftheriou, B. Fitch, J. Gagliano, A. Gara, R. Germain, M. E. Giampapa, M. Gupta, F. Gustavson, S. Hall, R. A. Haring, D. Heidel, P. Heidelberger, L. M. Herger, D. Hoenicke, R. D. Jackson, T. Jamal-Eddine, G. V. Kopcsay, A. P. Lanzetta, D. Lieber, M. Lu, M. Mendell, L. Mok, J. Moreira, B. J. Nathanson, M. Newton, M. Ohmacht, R. Rand, R. Regan, R. Sahoo, A. Sanomiya, E. Schenfeld, S. Singh, P. Song, B. D. Steinmacher-Burow, K. Strauss, R. Swetz, T. Takken, P. Vranas, T. J. C. Ward, J. Brown¹, T. Liebsch¹, A. Schram¹, G. Ulsh¹

IBM TJ Watson Research, Yorktown Heights, NY / ¹IBM Enterprise Server Group

System-on-a-chip technology allows a level of integration that can be leveraged to develop inexpensive high-performance, low-power computing nodes. When used in aggregate, this approach promises to challenge conventional supercomputer architectures in the high-performance computing arena. Systems under consideration reach into the hundreds of thousand nodes per machine. Architecture for these systems are described.

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J. Smith

12.2 Dynamic Microarchitecture Adaptation via Co-Designed Virtual Machines

James E. Smith, Ashutosh S. Dhodapkar

Department of Electrical and Computer Engineering,
University of Wisconsin, Madison, WI

Co-designed virtual machines provide hardware designers with a hidden layer of software that can be used to manage configurable hardware units. A reconfiguration algorithm based on a mechanism for identifying recurring program phases provides power savings in caches and predictors up to 60%, without significantly affecting performance.

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J. Rabaey

12.3 PicoRadios for Wireless Sensor Networks: The Next Challenge in Ultra-Low-Power Design

Jan M. Rabaey, Josie Ammer, Tufan Karalar, Suetfei Li, Brian Otis, Mike Sheets, Tim Tuan¹

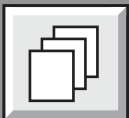
Univ. of California Berkeley, CA, ¹Xilinx Inc

Challenges and opportunities in design of integrated wireless sensor and actuator nodes, to be used in self-configuring ad-hoc networks, are described. To be viable, the node must be smaller than a couple of mm³, cost <\$1, and consume <100μW, allowing for energy scavenging from the environment.

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M. Gill

12.4 Ovonic Unified Memory - A High-Performance Nonvolatile Memory Technology for Stand-Alone Memory and Embedded Applications

Manzur Gill¹, Tyler Lowrey², John Park³

¹Intel Corporation, Santa Clara CA, ²Ovonyx Corp., Santa Clara CA

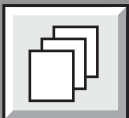
³Azalea Corp., Santa Clara CA

Development status of Ovonic unified memory (OUM), a phase-change non-volatile semiconductor memory technology is discussed. Using 0.18 μ m 3V CMOS, cells from 5F² to 8F² are built in a charge-pump-free 4Mb development vehicle. Direct overwrite, 10ns reset times, 50ns set times, and 1.0x10¹² cycling are achieved. Ten-year data retention is projected at 120°C.

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S. Goldstein

12.5 Digital Logic Using Molecular Electronics

Seth Copen Goldstein, Dan Rosewater

School of Computer Science, Carnegie Mellon University, Pittsburgh, PA

A reconfigurable architecture is based on chemically-assembled electronic nanotechnology (CAEN). A molecular latch based on molecular RTDs provides I/O-isolation, voltage restoration, and fan-out using only 2-terminal devices.

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K. Uchida

12.6 Programmable Single-Electron Transistor Logic for Low-Power Intelligent Si LSI

Ken Uchida, Junji Koga, Ryuji Ohba, Akira Toriumi¹

Advanced LSI Tech Lab, Toshiba Corp, Yokohama, Japan

¹Now at The University of Tokyo, Tokyo, Japan

Room-temperature-operating single-electron devices work not only as single-electron transistors (SETs) but also as nonvolatile single-electron memories. It is demonstrated that the combination of Coulomb oscillations with the nonvolatile memory functions offers high programmability for LSIs. The power and delay of a programmable SET logic are estimated.

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T. Hanyu

12.7 Ferroelectric-Based Functional Pass-Gate for Fine-Grain Pipelined VLSI Computation

¹Takahiro Hanyu, ¹Hiromitsu Kimura, ¹Michitaka Kameyama,
²Yoshikazu Fujimori, ²Takashi Nakamura, ²Hidemi Takasu

¹Graduate School of Information Sciences, Tohoku University, Sendai, Japan,

²Semiconductor Research and Development Headquarters, Rohm Co., Ltd., Kyoto, Japan

The state-transition scheme of remnant polarization in a ferroelectric capacitor performs storage and switching functions simultaneously with a functional pass-gate. As an example of fine-grain pipelined VLSI computation, a 250MHz 54x54b pipelined multiplier has 2.5W estimated power dissipation in a 0.6 μ m ferroelectric/CMOS technology.

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M. Igarashi

12.8 A Diagonal Interconnect Architecture and Its Application to RISC Core Design

Mutsunori Igarashi¹, Takashi Mitsuhashi¹, Andy Le², Shardul Kazi², Yang-Trung Lin³, Aki Fujimura³, Steve Teig³

¹Toshiba Corporation, Tokyo Japan, ²ArTile Microsystems, Inc., San Jose, CA

³Simplex Solutions, Inc., Sunnyvale, CA

Applying a design methodology based on an interconnect architecture characterized by pervasive use of diagonal wiring to a 128b RISC processor core design results in 19.8% path delay reduction and 10% area reduction, compared to the conventional orthogonal interconnect architecture.

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F. Henkel

13.1 A 1MHz-Bandwidth Second-Order Continuous-Time Quadrature Bandpass Sigma-Delta Modulator for Low-IF Radio Receivers

Frank Henkel¹, Ulrich Langmann¹, Andre Hanke², Stefan Heinen²,
Elmar Wagner²

¹Ruhr-Universität Bochum, Lehrstuhl für Elektronische Bauelemente, Bochum, Germany

²Infineon Technologies AG, Design Center Düsseldorf, Düsseldorf, Germany

A 2nd-order continuous-time quadrature bandpass $\Sigma\Delta$ modulator with 1MHz IF clocked at 100MHz digitizes I and Q inputs with SNDR of 56.2dB for 1MHz bandwidth inputs. The 0.65 μ m BiCMOS chip consumes 21.8mW at 2.7V, and operates with a clock-frequency range of 25-100MHz.

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R. Schreier

13.2 A 50mW Bandpass $\Sigma\Delta$ ADC with 333kHz BW and 90dB DR

Richard Schreier, Jennifer Lloyd, Lawrence Singer, Donald Paterson, Michael Timko, Michael Hensley, Gregory Patterson, Kevin Behel, James Zhou, William J. Martin¹

Analog Devices, Inc., Wilmington MA, ¹Motorola, Ft. Lauderdale, FL

A mixer plus multi-bit bandpass $\Sigma\Delta$ ADC achieves 89dB and 77dB SNR in 35kHz and 333kHz bandwidths at 273MHz IF while consuming 16mA from a 3V supply. The 6th-order ADC combines continuous-time LC and active RC resonators with a discrete-time switched-capacitor resonator, and includes AGC capability.

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T. Salo

13.3 A Dual-Mode 80MHz Bandpass $\Delta\Sigma$ Modulator for a GSM/WCDMA IF-Receiver

T. Salo¹, T. Hollman², S. Lindfors³, K. Halonen¹

¹Helsinki University of Technology, Finland, ²Texas Instruments, Finland

³Aalborg University, Denmark

A band-pass $\Delta\Sigma$ modulator operating at 80MHz combines frequency down-conversion with A/D conversion. The two SC resonators are implemented using a single opamp. A single-bit quantizer and feedback is used for GSM, but 4b quantizer is used for WCDMA. Measured peak SNRs are 80dB for 270kHz B/W (GSM), and 48dB for 3.84MHz B/W (WCDMA).

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R. Jiang

13.4 A 1.8V 14b $\Delta\Sigma$ A/D Converter with 4MSamples/s Conversion

Ruoxin Jiang, Terri S. Fiez¹

Maxim Integrated Products, Hillsboro, OR, ¹Oregon State University, Corvallis, OR

A fifth-order single-stage $\Delta\Sigma$ modulator achieves 14b resolution with 8x OSR and 4MHz conversion bandwidth in a 1.8V 0.18 μ m CMOS process. The DC gain of the internal op amps is 43dB. It occupies 1.3X2.2mm² and consumes 102mW analog power and 47mW digital power.

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R. Van Veldhoven

13.5 A 3.3mW $\Sigma\Delta$ Modulator for UMTS in 0.18 μm CMOS with 70dB Dynamic Range in 2MHz Bandwidth

Robert van Veldhoven, Kathleen Philips, Brian Minnis¹

Philips Research Laboratories, Eindhoven, The Netherlands

¹Redhill, United Kingdom

A 4th-order continuous-time, $\Sigma\Delta$ modulator with 1.5b quantizer and feedback DAC for a UMTS receiver has 70dB DNR in a 2MHz band and -74dB THD at full scale. An IC including two modulators, a PLL, and an oscillator dissipates 11.5mW at 1.8V. Active area is 0.41mm² in 0.18 μm , 1 poly 5-metal-layer CMOS technology.

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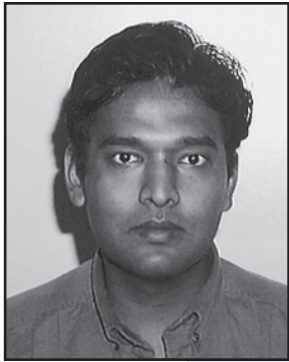


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S. Gupta

13.6 A 64MHz $\Sigma\Delta$ ADC with 105dB IM3 Distortion using a Linearized Replica Sampling Network

Sandeep K. Gupta, Todd L. Brooks, Victor Fong

Broadcom Corp, Irvine, CA

A $\Sigma\Delta$ ADC with 105dB distortion up to 1.5MHz signal bandwidth uses a linear sampling network in a 2-1-1 modulator. Operating at 64MHz clock frequency, the measured SNR in a 1.1MHz bandwidth is 88dB. The area, including bypass capacitors, is 2.6mm². The power consumed is 230mW, including references and decimation filter.

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E. Liu

13.7 A 3V $\Delta\Sigma$ Receiver with Sampling Rate Enhancement for CDMA Baseband Processor IC

Ed Liu, Min Chen, Mingde Pan

LSI Logic, Milpitas, CA

A 3V $\Delta\Sigma$ CDMA baseband receiver has a 4th-order single-loop modulator that enhances the effective sampling rate without increasing the actual rate, achieves 62dB DR, consumes 22mW, and occupies 1.3mm² in 0.25 μ m CMOS. The 8M transistor 10.5x10.5mm² chip integrates receiver, transmitter, voice codec, 10b ADC and DAC, PLL, 32kHz oscillator, two DSP, memory, and ARM.

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S. Dow

14.1 A Dual-Band Direct-Conversion/VLIF Transceiver for 50GSM/GSM/DCS/PCS

Stephen Dow, Brian Ballweber, Ling-Miao Chou, David Eickbusch, Jim Irwin, Gary Kurtzman, Praveen Manapragada, David Moeller, Jeyanandh Paramesh, Greg Black, Robert Wollscheid, Ken Johnson

Motorola Inc., Austin TX; Libertyville IL

The transceiver IC, in SiGe:C BiCMOS, contains dual LNAs, dual quadrature mixers, baseband filtering, RX and TX VCOs, and transmit buffers. The IC has GSM band performance of 67.5dB gain, 2.3dB NF, +49dBm IIP2, -9dBm IIP3 50dB image rejection, and TX noise $<-162\text{dBc/Hz}$ at 20MHz.

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R. Magoon

14.2 A Single-Chip Quad-Band (850/900/1800/1900MHz) Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer

Alyosha Molnar, Rahul Magoon, Geoffrey Hatcher, Jeffrey Zachan, Woogeun Rhee, Morten Damgaard, William Domino, Nooshin Vakilian

Conexant Systems Inc., Newport Beach CA

A monolithic IC integrates all the active RF functions of a quad band GSM handset except for the PA. A direct-conversion receiver (900MHz NF 3.0dB, IIP2 +65dBm) and an up-conversion loop transmitter (900MHz spectrum at 400kHz -65dBc, phase noise at 20MHz -164dBc/Hz) use a fractional-N PLL and fully-integrated transmit and UHF VCOs.

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V. Aparin

14.3 A Highly-Integrated Tri-Band/Quad-Mode SiGe BiCMOS RF-to-Baseband Receiver for Wireless CDMA/WCDMA/AMPS Applications with GPS Capability

Vladimir Aparin, Pete Gazzo, Jianjun Zhou, Bo Sun, Sandor Szabo, Eric Zeisel, Tony Segoria, Steven Ciccarelli, Charlie Persico, Chiewcharn Narathong, Ravi Sridhara

Qualcomm Inc., San Diego, CA

A 0.5 μ m SiGe BiCMOS single-chip receiver integrates three front-ends (LNA, RF-to-IF mixer, VGA) for the cellular, PCS/IMT and GPS frequency bands, a shared I/Q demodulator, IF VCO, and UHF LO buffers. It has 2.0dB NF and -0.6dBm IIP3 in the cellular CDMA mode and 2.3dB NF and -7dBm IIP3 in the PCS mode with <150mW at 3V.

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J. Vankka

14.4 A GSM/EDGE/WCDMA Modulator with On-Chip D/A Converter for Base Station

Jouko Vankka, Jaakko Ketola, Olli Väänänen, Johan Sommarek, Marko Kosunen, Kari Halonen

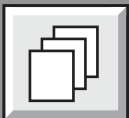
Helsinki University of Technology, Espoo, Finland

A modulator with a 14b on-chip D/A converter occupies 22.09mm² in 0.35μm CMOS and dissipates 1.7W at 3.3V with a 110MHz clock. A digital programmable up/down unit enables power ramping on a time-slot basis. The modulator fulfills the spectrum, phase and EVM specifications of GSM, EDGE and WCDMA.

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S. Embabi

14.5 A Highly-Integrated SiGe BiCMOS WCDMA Transmitter IC

**Abdellatif Bellaouar, Michel Frechette, Ahmed R. Fridi,
Sherif H.K. Embabi**

RF Design Group, Texas Instruments Inc., Dallas, TX

A highly-integrated SiGe BiCMOS WCDMA transmitter IC consists of VHF, UHF chains, and synthesizers. At 6dBm output power, it consumes 79mA at 2.7V, with a 5% rms EVM and -42dBc ACLR at 5MHz offset. In-band and receive-band output noise are -128 and -135dBm/Hz, respectively. Fully integrated PLLs use on-chip VCO tanks and require no off-chip loop filters.

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D. Manstretta

14.6 A 0.18 μ m CMOS Direct-Conversion Receiver Front-End for UMTS

**Danilo Manstretta, Rinaldo Castello, Francesco Gatta,
Paolo Rossi, Francesco Svelto**

University of Pavia, Pavia, Italy

An IC contains LNA, quadrature mixers and VGAs, realized in 0.18 μ m CMOS. It has +48.8dBm IIP2, -6dBm in band IIP3 (-2dBm out of band IIP3), 6.2dB DSB NF integrated in a 10kHz-1.92MHz band and draws 15mA from a 1.8V supply.

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D. Pfaff

14.7 An 18mW 1800MHz Quadrature Demodulator in 0.18 μ m CMOS

D. Pfaff, Q. Huang

Integrated Systems Laboratory, ETH Zurich, Switzerland

A demodulator consists of a 3.6GHz VCO, a 3.8mA current-mode divider for the I/Q generation, and two single-ended input double-balanced mixers. The IC consumes 10mA at 1.8V, and has -114dBc phase noise at 100kHz offset, 40dB image rejection, 14dB DSB noise figure and 8.5dBm IIP3.

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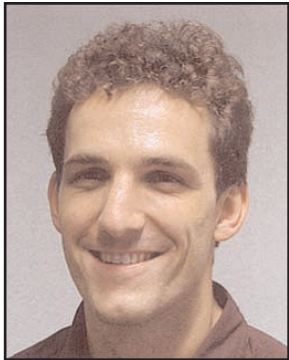


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G. Brenna

14.8 A 2GHz Direct-Conversion WCDMA Modulator in 0.25 μ m CMOS

Gabriel Brenna, David Tschopp, Dirk Pfaff, Qiuting Huang

Integrated Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Switzerland

A modulator IC delivers -8dBm maximum output power. Gain is programmable over a 78dB range in 1dB steps with 0.3dB accuracy. Consuming 41mA from a 2.5V supply, the modulator achieves a 15dBm OIP3, 50dBm OIP2, 36dB rejection of unwanted sideband, 47dB carrier suppression and -148dBc/Hz out-of-band-noise.

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M. Green

15.1 OC-192 Transmitter in Standard 0.18 μ m CMOS

**Michael M. Green¹, Afshin Momtaz, Kambiz Vakilian, Xin Wang,
Keh-Chee Jen, David Chung, Jun Cao, Mario Caresosa,
Armond Hairapetian, Ichiro Fujimori, Yijun Cai**

Broadcom Corp., Irvine, CA, USA, ¹now with University of California, Irvine

A fully integrated SONET OC-192 transmitter IC using a standard CMOS process consists of an input data register, FIFO, CMU, and 16:1 multiplexer to give a 10Gb/s serial output. A higher FEC rate, 10.7Gb/s, is supported. This chip, using a 0.18 μ m process, exceeds SONET requirements, dissipating 450mW.

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J. Cao

15.2 OC-192 Receiver in Standard 0.18 μ m CMOS

**Jun Cao, Afshin Momtaz, Kambiz Vakilian, Michael Green¹,
David Chung, Keh-Chee Jen, Mario Caresosa, Ben Tan,
Ichiro Fujimori, Armond Hairapetian**

Broadcom Corp., Irvine, CA, ¹now with University of California, Irvine, CA

A fully integrated OC-192 multi-rate (9.95Gb/s - 10.71Gb/s) receiver uses standard 0.18 μ m CMOS. The circuit consists of an input amplifier, CDR, 1:16 demux and 18 LVDS drivers. The chip exceeds SONET jitter tolerance spec by >100%. Recovered 10Gb/s clock jitter is <4mUI(rms). The input sensitivity is <50mV with 870mW at 1.8V.

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H. Noguchi

15.3 A 9.9G-10.8Gb/s Rate-Adaptive Clock and Data-Recovery with No External Reference Clock for WDM Optical Fiber Transmission

H. Noguchi, T. Tateyama, M. Okamoto, H. Uchida,
M. Kimura, K. Takahashi

Fiber Optic Devices Division, NEC Corporation, Kawasaki, Japan

A 9.9-10.8Gb/s rate adaptive clock and data recovery circuit with 1:16 DMUX are integrated in 0.5 μ m SiGe BiCMOS. A dual-input voltage-controlled oscillator incorporates a fast and a slow tracking loop with a DC gain enhancer. The chip exhibits 2mUIrms jitter generation and 0.45UIpp jitter tolerance in a 4-80MHz range. Power dissipation is 1.45W from a 3.3V supply.

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J. Rogers

15.4 A 10Gb/s CDR/DEMUX with LC Delay Line VCO in 0.18 μ m CMOS

Jonathan E. Rogers, John R. Long

Department of Electrical and Computer Engineering, University of Toronto, ON, Canada

A monolithic 10Gb/s clock/data recovery and 1:2 demultiplexer is implemented in 0.18 μ m CMOS. The quadrature LC delay line oscillator has 110MHz tuning range and 60MHz/V sensitivity to power-supply pulling. The circuit meets SONET OC-192 requirements with 1ps rms measured jitter. The 1.9x1.5mm² IC consumes 285mW from a 1.8V supply.

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S. Lee

15.5 A 5Gb/s 0.25 μ m CMOS Jitter-Tolerant Variable-Interval Oversampling Clock/Data Recovery Circuit

Sang-Hyun Lee, Moon-Sang Hwang, Youngdon Choi, Sungjoon Kim, Yongsam Moon, Bong-Joon Lee, Deog-Kyoon Jeong, Wonchan Kim, Young June Park, Gi-Jung Ahn*

Seoul National University, Seoul, Korea, *Silicon Image, Sunnyvale, CA

A variable-interval oversampling clock/data recovery circuit (CDR) provides robust operation under varying jitter conditions. An eye-measuring loop in the CDR enables data recovery at maximum eye-opening, responding to the amount and shape of jitter. The CDR in 0.25 μ m CMOS shows $<10^{-13}$ BER for 2^7-1 PRBS at 5GBaud.

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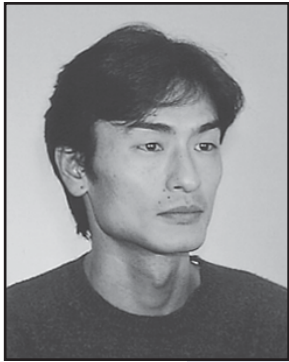


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T. Takeshita

15.6 A 622Mb/s Fully-Integrated Optical IC with a Wide Range Input

T. Takeshita, T. Nishimura

Sony Corporation, Atsugi, Kanagawa, Japan

An optical receiver IC for 622Mb/s that integrates transimpedance amplifier, post amplifier, and clock recovery uses a BiCMOS process. The one-chip receiver achieves dynamic range sensitivity from -29.4 to 0dBm. A PLL circuit without reference-clock tolerates input with duty-cycle distortion from 70 to 130%.

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M. Meghelli

15.7 50Gb/s SiGe BiCMOS 4:1 Multiplexer and 1:4 Demultiplexer for Serial-Communication Systems

Mounir Meghelli, Alexander V. Rylyakov, Lei Shan

IBM T. J. Watson Research Center, Yorktown Heights, NY

SiGe BiCMOS 4:1 multiplexer and 1:4 demultiplexer ICs targeting SONET OC-768 applications are packaged to enable bit-error-rate testing by connecting their serial interfaces. Operation is error-free for both circuits at data rates $>50\text{Gb/s}$ and -3.6V supply.

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M. Fukaishi

16.1 A 100Gb/s Transceiver with GND-VDD Common-Mode Receiver and Flexible Multi-Channel Aligner

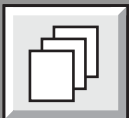
Kenichi Tanaka, Muneo Fukaishi, Masahiro Takeuchi, Nobuhide Yoshida, Kouichirou Minami, Kouichi Yamaguchi, Hiroyuki Uchida, Yasuyuki Morishita, Takehiko Sakamoto, Tomoyuki Kaneko, Masaaki Soda, Masakazu Kurisu, Takanori Saeki
NEC Corp., Kanagawa, Japan

A 5Gb/s 20-channel transceiver uses 0.13 μ m 1.5V CMOS technology. The sampling amplifier recovers ± 100 mV 90ps data over 0-1.5V common-mode range. A flexible multi-channel aligner and full-digital CDR architecture are used.

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A. Mäntyniemi

16.2 An Integrated 9-Channel Time Digitizer with 30ps Resolution

Antti Mäntyniemi, Timo Rahkonen, Juha Kostamovaara

University of Oulu, Finland, Department of Electrical Engineering, Electronics Laboratory

An integrated 9-channel time digitizer with 30ps rms resolution, 496 μ s range, and 50mW power consumption in 0.6 μ m CMOS uses a three-stage delay line interpolation and delay-generation principle that divides the 66MHz clock period into 512 bins using only 45 delay elements.

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J. Kim

16.3 Adaptive Supply Serial Links with Sub-1V Operation and Per-Pin Clock Recovery

Jaeha Kim, Mark A. Horowitz

Computer Systems Laboratory, Stanford University, Stanford, CA

Adaptive power-supply regulation is extended to serial links, by using 5:1 multiplexing and low-voltage transceivers for power saving, and by scaling link properties with bit rate, especially in per-pin clock recovery PLL/DLLs. The serial link operates at 0.45-3.5Gb/s for 0.9-2.5V supply and dissipates 9.2-197mW.

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S. Narendra

16.4 1.1V 1GHz Communications Router with On-Chip Body Bias in 150nm CMOS

Siva Narendra, Matthew Haycock, Venkatesh Govindarajulu, Vasantha Erraguntla, Howard Wilson, Sriram Vangal, Amaresh Pangal, Erik Seligman, Raj Nair, Ali Keshavarzi, Bradley Bloechel, Gregory Dermer, Randy Mooney, Nitin Borkar, Shekhar Borkar, Vivek De

Microprocessor Research Labs, Intel Corporation, Hillsboro, OR

A router chip, that incorporates on-chip forward body biasing capability with 2% area overhead, achieves 1GHz operation at 1.1V supply in a 150nm logic technology, compared to 1.25V required for the original design having no body bias. Switching power is 23% less and chip leakage is reduced by 3.5x in standby mode by withdrawing forward bias.

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R. Holzer

16.5 A 1V CMOS PLL Designed in High-Leakage CMOS Process Operating at 10-700MHz

Reuven Holzer

Analog Devices Inc., DSP Design Center, Herzlia, Israel

A PLL uses 0.13 μ m logic process where leakage currents are high. The loop capacitor is implemented by a structure of poly and 9 metal layers. The VCO is implemented with common-mode feedback to compensate for leakage currents. Maximum VCO frequency is 1400MHz. Typical power is 7mW at 200MHz. RMS jitter is 25.4ps at 360MHz.

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M. Badaroglu

16.6 Methodology and Experimental Verification for Substrate Noise Reduction in CMOS Mixed-Signal ICs with Synchronous Digital Circuits

Mustafa Badaroglu^{1,2}, Marc van Heijningen¹, Vincent Gravot¹, John Compiet¹, Stéphane Donnay¹, Marc Engels¹, Georges Gielen³, Hugo De Man^{1,3}

¹IMEC, Leuven, Belgium, ²Also Ph.D. student at K.U. Leuven, Belgium

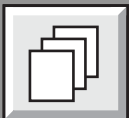
³K.U. Leuven, Belgium

An efficient substrate-noise-reduction technique for synchronous CMOS circuits shows >2x noise reduction with penalties of 3% area and 4% power increase in a 5k-gate synchronous CMOS circuit fabricated in a 0.35 μ m CMOS process on an epi-type substrate.

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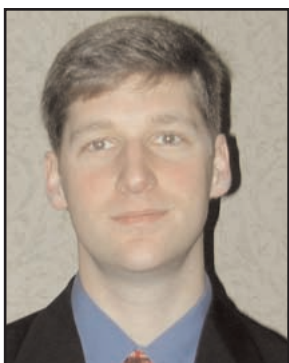


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M. Straayer

17.1 A Low-Noise Transformer-Based 1.7GHz CMOS VCO

Matt Straayer, Jose Cabanillas*, Gabriel M. Rebeiz

EECS Department, University of Michigan, Ann Arbor, MI, *Departament d'Electronica (SIC), University of Barcelona, Spain. Work done while at the University of Michigan

A low-noise transformer-based 0.35 μ m CMOS VCO operates at 1.7GHz. The VCO core consumes 4.5mA from 2.5V, and results in phase noise of -116, -137 and -142dBc/Hz at 100k, 600k and 1MHz from the carrier, respectively. The tuning range is 107MHz for 0-2.5V tuning voltage. The oscillator is based on a transformer-type resonator.

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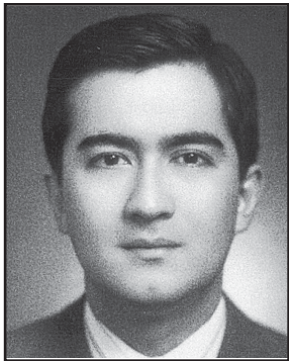


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R. Aparicio

17.2 A CMOS Differential Noise-Shifting Colpitts VCO

Roberto Aparicio, Ali Hajimiri

California Institute of Technology, Pasadena, CA

A $0.35\mu\text{m}$ VCO uses current switching to increase voltage swing, lower phase noise by cyclostationary noise alignment, and improve start-up reliability. A CMOS VCO in a 3-metal, $0.35\mu\text{m}$ process has -139dBc/Hz phase noise at 3MHz offset from a 1.8GHz carrier and 30% of continuous tuning using inductors with Q of 6 and 4mA dc current.

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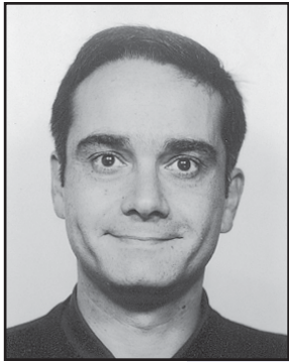


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P. Andreani

17.3 A Low-Phase-Noise Low-Phase-Error 1.8GHz Quadrature CMOS VCO

Pietro Andreani

Department of Electrosience, Lund University, Sweden

A 1.8GHz quadrature VCO in standard 0.35 μ m CMOS with three metal layers shows -140dBc/Hz or less phase noise across an 18% tuning range, while drawing 25mA from a 2V power supply. The quadrature phase error between the VCO outputs is at most 0.25 $^\circ$.

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D. Hitko

17.4 Adaptive Biasing of a 5.8GHz CMOS Oscillator

Donald A. Hitko, Charles G. Sodini

MIT Microsystems Technology Laboratories, Cambridge, MA

A key concept for VCOs in next-generation RF links is to allow phase noise performance to be scaled back to save power in times of reduced demand. A 5.8GHz VCO and biasing circuitry in 0.5 μ m CMOS have performance adjustable from -107dBc/Hz (1MHz offset) with 6.2mW dissipated to -121dBc/Hz using 70mW.

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T. Sowlati

17.5 A 2.4GHz 0.18 μ m CMOS Self-Biased Cascode Power Amplifier with 23dBm Output Power

Tirdad Sowlati, Domine Leenaerts¹

Philips Research-USA, Briarcliff Manor, NY

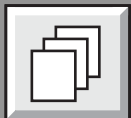
¹Philips Research, Eindhoven, the Netherlands

A two-stage self-biased cascode power amplifier in 0.18 μ m CMOS process for Class 1 Bluetooth application provides 23dBm output power with 31dB gain and 42% PAE at 2.4GHz. The power amplifier die occupies 0.46mm².

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P. Nagle

17.6 A Wideband Linear Amplitude Modulator for Polar Transmitters Based on the Concept of Interleaving Delta Modulation

Pierce J. Nagle¹, David P. Burton¹, Eugene P. Heaney²,
Finbarr J. McGrath³

¹University of Limerick, Ireland, ²M/A-COM, Ireland, ³M/A-COM, USA

A wideband amplitude modulator for use with an RF polar transmitter is based on interleaving delta modulation to improve linearity and reduce switching loss, filter size, and EMI. A 0.35 μ m CMOS 0.35mm² chip verifies the iDM concept.

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K. Ohata

17.7 Wireless 1.25Gb/s Transceiver Module at 60GHz-Band

Keiichi Ohata, Kenichi Maruhashi, Masaharu Ito, Shuya Kishimoto, Kazuhiro Ikuina¹, Takeya Hashiguchi¹, Nobuaki Takahashi², Shunichi Iwanaga³

Photonic and Wireless Devices Research Labs., NEC Corporation, Otsu, Japan,

¹Functional Materials Research Labs., NEC Corporation, Kawasaki Japan

²NEC Engineering Ltd., Kawasaki Japan, ³NEC Kansai Ltd., Otsu Japan

A 1.25Gb/s 60GHz-band compact transceiver module uses ASK modulation. CPW MMICs and planar filters are flip-chip mounted in TX and RX LTCC MCMs. The transmitter exhibits 9.6dBm output power. The receiver shows -50dBm minimum received power for 1.25Gb/s error-free transmission. The transceiver module is 82x53x7mm³ (30cc).

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M. Tiebout

17.8 A 1V 51GHz Fully-Integrated VCO in 0.12 μ m CMOS

Marc Tiebout, Hans-Dieter Wohlmuth, Werner Simbürger

Infineon Technologies AG, Corporate Research, Munich, Germany

A fully integrated 51GHz VCO is implemented in 0.12 μ m standard CMOS with 6 metal levels. Core power consumption is 1mW at 1V supply due to the optimized high-inductance tank. The tuning range is 1.4GHz. Measured phase noise is -85dBc/Hz at 1MHz offset.

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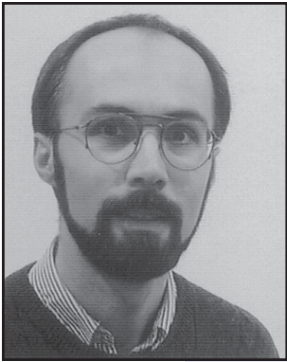


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H. Knapp

17.9 25GHz Static Frequency Divider and 25Gb/s Multiplexer in 0.12 μ m CMOS

Herbert Knapp, Hans-Dieter Wohlmuth, Martin Wurzer, Mira Rest

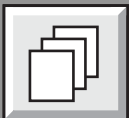
Infineon Technologies AG, Corporate Research, Munich, Germany

A static 2:1 frequency divider operating up to 25.4GHz at 41mA and a 25Gb/s 2:1 multiplexer at 29mA implemented in current-mode logic have differential 50 Ω inputs and outputs. They are fabricated in a 0.12 μ m CMOS process and operate from a 1.5V supply.

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G. Gomez

18.1 A 1.5V 2.4/2.9mW 79/50dB DR $\Sigma\Delta$ Modulator for GSM/WCDMA in a 0.13 μ m Digital Process

Gabriel Gomez, Baher Haroun

Texas Instruments, Inc., Dallas, TX, USA

A 2nd order multi-level $\Sigma\Delta$ A/D converter for low-power multi-standard wireless receivers, in a single-poly 0.13 μ m digital CMOS process, has 79/50dB dynamic range for GSM/WCDMA. The 0.2mm² chip consumes 2.4/2.9mW at 1.5V.

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J. (H.-C.) Lin

18.2 An Embedded 0.8V/480 μ W 6b/22MHz Flash ADC in 0.13 μ m Digital CMOS Process using Nonlinear Double-Interpolation Technique

Jerry (Heng-Chih) Lin, Baher Haroun

Texas Instruments Inc., Dallas, TX

For high-data-rate wireless communication, a 0.8V 480 μ W 6b 22MSample/s flash-interpolation ADC is fabricated in 0.13 μ m digital CMOS. The circuit achieves 33dB SNDR and 47dB SFDR using a nonlinear double-interpolation technique.

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J. Sauerbrey

18.3 A 0.7V MOSFET-Only Switched-Opamp $\Sigma\Delta$ Modulator

**Jens Sauerbrey¹, Thomas Tille², Doris Schmitt-Landsiedel²,
Roland Thewes¹**

¹Infineon Technologies AG, Corporate Research, Munich, Germany, ²Technical University of Munich, Institute for Technical Electronics, Munich, Germany

A 0.7V MOSFET-only switched-opamp $\Sigma\Delta$ modulator for speech applications achieves 67dB SNDR, and 75dB dynamic range. The circuit, occupying 0.08mm² in 0.18 μ m CMOS, does not use voltage boosting or low- V_T devices. All capacitors are compensated MOS devices.

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S. Kulhalli

18.4 A 30mW 12b 21MSample/s Pipelined CMOS ADC

Suhas Kulhalli, Visvesvaraya Penkota, Ravishankar Asv

Texas Instruments Inc., Bangalore, India

A 0.6 μ m double-poly CMOS 12b ADC uses a number of different techniques to obtain low power. The ADC achieves 68dB SNR at 21MSample/s, consuming 30mW at 2.7V. Die area is 2.56mm².

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M. Waltari

18.5 A Self-Calibrated Pipeline ADC with 200MHz IF-Sampling Frontend

Mikko Waltari, Lauri Sumanen, Tuomas Korhonen, Kari Halonen

Electronic Circuit Design Laboratory, Helsinki University of Technology, Finland

A 13b 50MSample/s pipeline ADC with digital self-calibration and IF-sampling frontend, using a 0.35 μ m BiCMOS process, achieves 76.5dB SFDR at 194MHz input. The chip occupies 6mm² and dissipates 715mW from a 2.9V supply.

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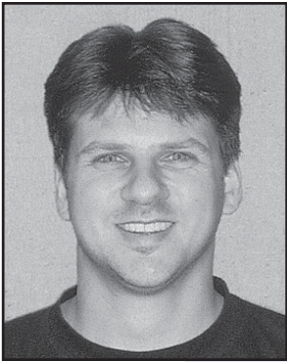


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R. Reutemann

18.6 A 33mW 14b 2.5MSample/s $\Sigma\Delta$ A/D Converter in 0.25 μ m Digital CMOS

Robert Reutemann, Pio Balmelli, Qiuting Huang

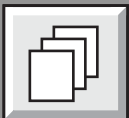
Integrated Systems Laboratory, ETH Zürich, Zürich, Switzerland

The IC consists of a 5th-order single-loop tri-level $\Sigma\Delta$ modulator and a multistage digital filter. Measured dynamic range is 86dB over 1MHz bandwidth. With 79dB peak SNDR, the chip consumes 33mW and occupies 1.5mm².

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J. W. Pierdomenico

19.1 A 744mW Adaptive Supply Full-Rate ADSL CO Driver

John Pierdomenico, Scott Wurcer, Bob Day

Analog Devices Inc., Wilmington, MA

A $\pm 6V$ ADSL CO driver delivers 20.4dBm power into a 100Ω load with 5.3 crest factor using internally pumped power supplies. In a 1:1.1 transformer reference design, $1E-08$ BER is measured while driving 8.16Mb/s down a 6.5kft line. Data rates up to 8Mb/s are measured. The device uses a 26V SOI bipolar process with 744mW of total supply.

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F. Sabouri

19.2 A 740mW ADSL Line Driver for Central Office with 75dB MTPR

Faramarz Sabouri, Reza Shariatdoust

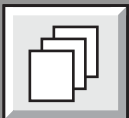
Analog Devices, Somerset, NJ

A bipolar ADSL line driver for central office achieves 75dB MTPR. Employing a single-active-termination topology, it has 710mW total dissipation including 20.4dBm delivered to the line. Class-AB biasing makes the 4mA quiescent current independent of process, temperature, and supply variations.

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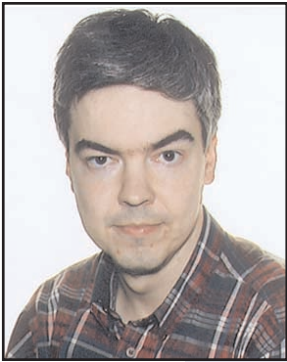


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M. Ingels

19.3 A 0.5 μ m CMOS Low-Distortion Low-Power Line Driver with Embedded Digital Adaptive Bias Algorithm for Integrated ADSL Analog Front-Ends

Mark Ingels, Sena Bojja, Patrick Wouters

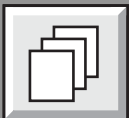
Alcatel Microelectronics, Zaventem, Belgium

A 5V 0.5 μ m CMOS line driver has distortion <-65 dB in the ADSL upstream band for a 4V peak-to-peak differential output swing on a 12.5 Ω load. The quiescent current is controlled digitally with a dedicated algorithm that corrects for offsets and process variations. The driver is integrated in a complete ADSL CPE analog front-end.

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H. Weinberger

19.4 A 1.8V 450mW VDSL 4-Band Analog Front End IC in 0.18 μ m CMOS

Hubert Weinberger, Andreas Wiesbauer, Martin Clara, Christian Fleischhacker, Thomas Pötscher, Berthold Seger

Infineon Technologies AG, Villach, Austria

A highly integrated AFE chip for VDSL-4band in 0.18 μ m CMOS draws 450mW from a single 1.8V supply. The 12MHz bandwidth transceiver employs an 11b ADC, a 12b DAC, automatically tuned anti-aliasing and reconstruction filters, and programmable gain amplifiers. Beside the basic transceiver circuitry, it also provides clock generation and wake-up circuitry on a 7.5mm² die.

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W. A. P. De Wilde

19.5 Analog Front End for DMT-Based VDSL

**W. De Wilde, N Scantamburlo¹, M. Combe², J. Van Leeuwe,
K. Doorackers, Y. Mazoyer², C. Renous², R. Petigny², A. Bonin²,
B. Bayracki¹, B. Belhi², E. Moons, J. Sevenhans**

Alcatel, Antwerpen, Belgium, ¹Padova, Italy, ²STMicroelectronics, Grenoble, France

A 12MHz 760mW analog front end for DMT-based VDSL integrates all active components except line driver in a single BiCMOS 0.35 μ m ASIC. When fully active, the ASIC dissipates 480mW at 3.3V supply, providing resolution equivalent to 12b without trimming.

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C. Ling

19.6 A Low-Power Integrated Tuner for Cable-Telephony Applications

**Curtis Ling, Raymond Montemayor, Alberto Cicalini, Kevin Wang,
Lars Jansson, Lars Mucke, Pushp Trihka, S.V. Kishore**

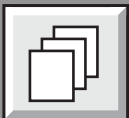
Silicon Wave, Inc., San Diego, CA

A fully-integrated dual-conversion tuner for cable telephony in a 27GHz 0.35 μ m SOI BiCMOS process receives signals from 200 to 880MHz and produces a 44MHz IF. The 13mm² IC has 7.3dB NF, <-78dBc/Hz total phase noise at 10kHz offset, spurs below 42dBc for 137 5dBmV channels, 60dB gain, and 68dB gain range, drawing 168mA from 3V.

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R. Preston

20.1 Design of an 8-wide Superscalar RISC Microprocessor with Simultaneous Multithreading

Ronald P. Preston, Roy W. Badeau, Daniel W. Bailey, Shane L. Bell, Larry L. Biro, William J. Bowhill, Daniel E. Dever, Stephen Felix, Richard Gammack, Valeria Germini, Michael K. Gowan, Paul Gronowski, Daniel B. Jackson, Shekhar Mehta, Shannon V. Morton, Jeffrey D. Pickholtz, Matthew H. Reilly, Michael J. Smith

Compaq Computer Corporation, Shrewsbury, MA

A 250M transistor microprocessor implements the Alpha instruction set and features 8-wide superscalar issue and simultaneous multithreading in a 0.125 μ m SOI process. Performance is estimated at over three times that of the previous design.

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Y-D. Bae

20.2 A Single-Chip Programmable Platform Based on a Multithreaded Processor and Configurable Logic Clusters

Young-Don Bae, Seong-II Park, Yongseok Yi, In-Cheol Park

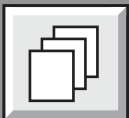
Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea

A configurable platform chip integrates most hardware blocks required in embedded system chip design, such as a 32b multithreaded RISC processor, configurable logic clusters, FIFO memories and control circuitry. The multithreaded processor has fast task switching and configurable logic are grouped into clusters for IP-based design.

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G. Konstadinidis

20.3 Implementation of a Third-Generation 1.1GHz 64b Microprocessor

Georgios Konstadinidis, Kevin Normoyle, Samson Wong, Sutikshan Bhutani, Harry Stuimer, Timothy Johnson, Alan Smith, Daniel Cheung, Fabrizio Romano, Shifeng Yu, Sung-Hun Oh, Victor Melamed, Shridar Narayanan, David Bunsey, Cong Khieu, Kevin J. Wu, Ralf Schmitt, Andy Dumlao, Massimo Sutura, Jade Chau, K. James Lin

Sun Microsystems, Palo Alto, CA

A third-generation 1.1GHz 64b microprocessor provides 1MB on-chip L2\$, 4GB/s off chip memory bandwidth and a 200MHz JBUS interface that supports 1 to 4 processors. The 90M transistor chip is implemented in a 7-level metal copper 0.13 μ m CMOS process and dissipates 53W at 1.3V and 1.1GHz

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K. J. Nowka

20.4 A 0.9V to 1.95V Dynamic Voltage-Scalable and Frequency-Scalable 32b PowerPC Processor

Kevin Nowka, Gary Carpenter, Eric Mac Donald¹, Hung Ngo, Bishop Brock, Koji Ishii², Tuyet Nguyen, Jeffrey Burns

IBM Austin Research Laboratory, ¹IBM Microelectronics Division, Austin, TX

²IBM Microelectronics Division, Yasu, Japan

A 32b PowerPC™ system-on-a-chip supporting dynamic voltage supply and dynamic frequency scaling operates from 366MHz at 1.8V and 600mW down to 150MHz at 1.0V and 53mW in a 0.18μm CMOS process. Maximum supply change without PLL relock is 10mV/μs. Processor state save/restore enables a deep-sleep state.

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M. Nakajima

20.5 A 400MHz 32b Embedded Microprocessor Core AM34-1 with 4.0GB/s Cross-Bar Bus Switch for SoC

Masaitsu Nakajima, Takao Yamamoto, Shinji Ozaki,
Tomohisa Sezaki, Tomochika Kanakogi, Takanori Furuzono,
Takeshi Sakamoto, Toshihisa Aruga, Masaya Sumita,
Masanori Tsutsumi, Akira Ueda, Takahiro Ichinomiya

Matsushita Electric Industrial Co. Ltd., Kyoto, Japan

A 32b RISC microprocessor core for Digital TV SoC occupies 14.8mm² in 0.13μm CMOS with six Cu layers. The core runs at 400MHz with 500mW average dissipation at 1.35V. The integrated 4.0GB/s 3 x 4 cross-bar bus switch improves sustained system performance efficiency by 1.75 times.

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S. D Naffziger

20.6 The Implementation of the Next-Generation 64b Itanium™ Microprocessor

Samuel D Naffziger, Gary Hammond¹

Hewlett Packard Corp. Fort Collins, CO, ¹Intel Corp. Santa Clara, CA

The processor incorporates over 220M transistors on a 465mm² die and operates at >1.2GHz with an 8-stage pipeline in a 0.18μm process. It has three levels of on-chip cache totaling over 3.3MB providing >32GB/s bandwidth at each level.

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A. Droitcour

21.1 0.25 μ m CMOS and BiCMOS Single-Chip Direct-Conversion Doppler Radar for Remote Sensing of Vital Signs

**Amy D. Droitcour, Olga Boric-Lubecke¹, Victor M. Lubecke¹,
Jenshan Lin²**

Center for Integrated Systems, Stanford University, Stanford, CA

¹Bell Labs, Lucent Technologies, Murray Hill, NJ, ²Agere Systems, Murray Hill, NJ

A fully integrated direct conversion Doppler radar detects heart and respiration movement at a distance of 50cm. The 1.6GHz transceiver is in both CMOS and BiCMOS, with each chip occupying 14mm² using a 0.25 μ m silicon processes. The effects on system sensitivity of phase noise at small offset frequencies with range correlation are assessed.

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R. Thewes

21.2 Sensor Arrays for Fully-Electronic DNA Detection on CMOS

**Roland Thewes¹, Franz Hofmann¹, Alexander Frey¹, Birgit Holzapfl¹,
Meinrad Schienle¹, Christian Paulus¹, Petra Schindler¹,
Gerald Eckstein², Christian Kassel², Manfred Stanzel²,
Reiner Hintsche³, Eric Nebling³, Jörg Albers³, Jörg Hassman⁴,
Jürgen Schüle⁴, Wolfgang Goemann⁵, Walter Gumbrecht²**

¹Infineon Technologies, Corporate Research, Munich, Germany, ²Siemens AG, Munich / Erlangen, Germany, ³Fraunhofer Gesellschaft, ISiT, Itzehoe, Germany
⁴November AG, Erlangen, Germany, ⁵Eppendorf Instrumente GmbH, Hamburg, Germany

A 16x8 DNA sensor array chip with fully electronic readout is based on an extended CMOS process. Requirements concerning the integration of bio-compatible interface-, sensor- and transducer-materials into standard-CMOS-environment and circuitry design issues are discussed.

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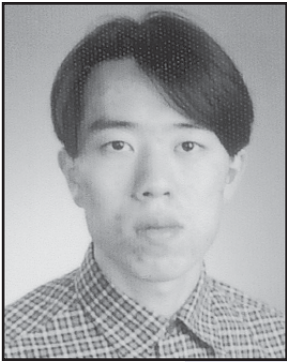


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K. Lee

21.3 A 500dpi Capacitive-Type CMOS Fingerprint Sensor with Pixel-Level Adaptive Image Enhancement Scheme

Kwang-Hyun Lee, Euisik Yoon

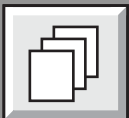
Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea

A 500dpi capacitive CMOS fingerprint sensor with pixel-level adaptation image enhancement uses virtually-grounded metal shields to suppress parasitic capacitances and capacitive switching networks to generate local threshold level. A 210x100 sensor in 0.6 μ m CMOS consumes 40mW at 5V supply.

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S. Shigematsu

21.4 A 500dpi 224x256Pixel Single-Chip Fingerprint Identification LSI with Pixel-Parallel Image Enhancement and Rotation Schemes and Rotation Schemes

Satoshi Shigematsu, Koji Fujii, Hiroki Morimura, Takahiro Hatano, Mamoru Nakanishi, Takuya Adachi, Namiko Ikeda, Toshishige Shimamura, Katsuyuki Machida¹, Yukio Okazaki, Hakaru Kyuragi¹

NTT Lifestyle and Environmental Technology Laboratories, Kanagawa, Japan

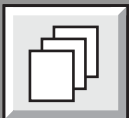
¹NTT Telecommunications Energy Laboratories, Kanagawa, Japan

A 500-dpi 224x256-pixel single-chip fingerprint identification LSI adapts the sensing circuit to a finger and performs pixel-parallel image processing and rotation in a pixel array. A test chip achieves 2ms 10mW sensing, 41ms 19.2mW identification, and practical identification accuracy at 2.5V, 5MHz.

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K. Najafi

21.5 Micromachined e-Jet for IC Chip Cooling

**Tsung-Kuan A. Chou, Khalil Najafi, Michael O. Muller¹,
Luis P. Bernal¹, Peter D. Washabaugh¹, Babak A. Parviz**

Center for Wireless Integrated MicroSystems

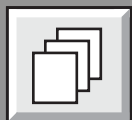
¹Aerospace Engineering Department, University of Michigan, Ann Arbor, MI

A micromachined acoustic ejector (MACE) chip contains electrostatically-driven Helmholtz resonators that generate small air jets. A 1.6x1.6cm² prototype contains 25 e-jets with 1m/s measured velocity. Results show that a 15-jet device located ~1cm above a 100°C surface dissipates >6W/m²K. Future generations are being designed with higher jet velocity.

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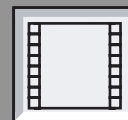
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M. Wu

21.6 Microelectromechanical Scanning Devices for Optical Networking Applications

**Ming C. Wu, Dooyoung Hah, Pamela R. Patterson,
Hiroshi Toshiyoshi¹**

Electrical Engineering Department, University of California, Los Angeles, CA

¹Institute of Industrial Science, University of Tokyo, Tokyo, Japan

The state-of-the-art of optical MEMS devices for optical networking applications is reviewed, and a scanning micromirror with angular vertical comb (AVC) actuators is introduced. The AVC scanner uses a single etching process and is completely self-aligned. It has 50% larger scan angle than conventional vertical comb devices. Resonant frequency is 630Hz.

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A. Ionescu

21.7 3-D Integrable Optoelectronic Devices for Telecommunications ICs

Paolo Dainesi, Adrian M. Ionescu, Luc Thévenaz, Kaustav Banerjee¹, Michel J. Declercq, Philippe Robert, Philippe Renaud, Philippe Fluckiger, Cyrille Hibert, Georges A. Racine

Swiss Federal Institute of Technology Lausanne (EPFL), Switzerland

¹Center for Integrated Systems, Stanford University, CA

3-D integrable SOI optoelectronic devices include telecommunication optical switches with 5MHz bandwidth and unbalanced Mach Zehnder interferometers for filtering. Thermal compensation provides efficient modulation over 100kHz-1MHz and addresses 3-D IC thermal issues.

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G. de Jong

21.8 A DC-to-250MHz Current Pre-Amplifier with Integrated Photo-Diodes in Standard CBiMOS, for Optical-Storage Systems

Gerben W. de Jong, Jozef R.M. Bergervoet, Johannes H.A. Brekelmans, Job F.P. van Mil¹

Philips, ¹Philips Optical Storage, Eindhoven, The Netherlands

An opto-electronic IC contains pre-amplifiers and integrated photo-diodes for optical-storage systems (CD, DVD, and DVR). The pre-amps exhibit $4.6\text{nV}/\sqrt{\text{Hz}}$ noise and the diodes have 0.25pF junction-capacitance. The IC uses a standard $0.6\mu\text{m}$ CBiMOS process for a high-performance low-cost solution.

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M. Ohashi

22.1 A 27MHz 11.1mW MPEG-4 Video Decoder LSI for Mobile Application

Masahiro Ohashi, Takashi Hashimoto, Shun-ichi Kuromaru, Masatoshi Matsuo, Toshihiro Mori-iwa, Mana Hamada, Yuji Sugisawa, Miki Arita, Hiroto Tomita, Masashi Hoshino, Hiroshi Miyajima, Tsuyoshi Nakamura, Ken-ichi Ishida, Tomoo Kimura, Yasuo Kohashi, Takahiro Kondo, Akihiko Inoue, Hitoshi Fujimoto, Kazuhiro Watada, Tarou Fukunaga, Takahiro Nishi¹, Hiroyuki Ito², Junji Michiyama

Matsushita Electric Industrial Co., Ltd., Fukuoka, ¹Osaka, Japan

²Matsushita Communication Industrial Co., Ltd., Kanagawa, Japan

A single-chip MPEG-4 video decoder LSI with integrated 896kb embedded SRAM frame buffer and embedded video display engine consumes 11.1mW at 27MHz operation. The chip achieves QCIF 15Hz H.263 and Simple@L1 decoding capability on 37.26mm² die using 0.18 μ m 1.5V quad-metal CMOS technology.

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H. Nakayama

22.2 A MPEG-4 Video LSI with an Error-Resilient Codec Core Based on a Fast Motion Estimation Algorithm

Hiroshi Nakayama, Toshiyuki Yoshitake, Hiroshi Komazaki, Yasuhiro Watanabe, Hisakatsu Araki, Kiyonori Morioka, Jiang Li, Liu Peilin, Shinhaeng Lee, Hajime Kubosawa, Yukio Otobe

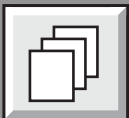
Fujitsu Laboratories Ltd., Kawasaki, Japan

An MPEG4 video codec core based on a scene-adaptive motion estimation algorithm is integrated into 5.296x5.296mm² die using 0.18 μ m quad-metal technology. The power dissipation during codec operation of the device is 131mW for QCIF format at 15 frames/s at 13.5MHz using a 1.5V supply.

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T. Yamada

22.3 A 133MHz 170mW 10 μ A Standby Application Processor for 3G Cellular Phones

T. Yamada, N. Irie, J. Nishimoto, Y. Kondoh, T. Nakazawa, K. Yamada, K. Tatezawa, T. Irita, S. Tamaki, H. Yagi, M. Furuyama, K. Ogura¹, H. Watanabe, R. Satomura, K. Hirose, F. Arakawa, T. Hattori, I. Kudo, I. Kawasaki, K. Uchiyama

Hitachi Ltd., Tokyo, Japan, ¹Hitachi ULSI Systems Co., Ltd., Tokyo, Japan

An application processor for 3G cellular phones, using 0.18 μ m CMOS technology, includes a single CPU and DSP core with an on-chip 128kB SRAM. It enables software-based 15frames/s MPEG-4 encoding of QCIF Simple @L1 at 70MHz and 140mW. Standby current of the processor is <10 μ A in a partially powered standby mode using separate power lines.

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H. Yamauchi

22.4 A 0.8W HDTV Video Processor with Simultaneous Decoding of Two MPEG2 MP@HL Streams and Capable of 30frames/s Reverse Playback

Hideki Yamauchi, Shigeyuki Okada, Kazuhiko Taketa, Yuh Matsuda, Tsugio Mori, Shin'ichiro Okada, Tsuyoshi Watanabe, Yasoo Harada, Morio Matsudaira, Yoshifumi Matsushita

Sanyo Electric Co., Ltd., Gifu, Japan

A HDTV video processor with decoding/display of two MPEG MP@HL streams and reverse playback with smooth 30frames/s without frame skip uses a 0.18 μ m 5-layer process in 6.86x6.86mm² and 5.7M transistors. It is for home multimedia and mobile TV applications. It operates at 135MHz and 0.8W at 1.8V.

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H. Okano

22.5 An 8-way VLIW Embedded Multimedia Processor built in 7-layer Metal 0.11 μ m CMOS Technology

Hiroshi Okano, Atsuhiko Suga, Tetsuyoshi Shiota, Yoshimasa Takebe, Yasuki Nakamura, Naoshi Higaki, Haruo Kimura, Hideo Miyake, Tomio Satoh, Ken-ichi Kawasaki, Ryuhei Sasagawa, Wataru Shibamoto, Mitsuru Sasaki, Naruyoshi Ando, Tomohiro Yamana, Isao Fukushi, Shin-ichirou Tago, Fumihiko Hayakawa, Teruhiko Kamigata, Satoshi Imai, Atsushi Satoh, Yasuaki Hatta², Noboru Nishimura³, Yoshimi Asada, Taizo Satoh¹, Takao Sukemura¹, Satoshi Ando, Hiromasa Takahashi

Fujitsu Laboratories Ltd., Fujitsu Ltd.¹, Fujitsu LSI Technology Ltd.², Fujitsu Devices Inc.³, Kanagawa, Japan

A 533MHz 2.5W 2132MIPS 12.8GOPS 2.1GFLOPS 8-way VLIW embedded multimedia processor occupies a 7.8x7.8mm² die in a 7-layer metal 0.11 μ m CMOS at 1.2V. VLIW, SIMD, dynamic branch prediction, non-aligned dual load/store mechanism and a crosstalk-aware design flow contribute to performance.

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G. Jackson

22.6 A Single-Chip Text-To-Speech Synthesis Device Utilizing Analog Non-Volatile Multi-Level Flash Storage

Geoff Jackson, Saleel V. Awsare, Ming-Bing Chang, Wen-Kuei Chen, Rodney Doan, Larry Gaddy, Peter Holzmann, Dan Kahn¹, Rick Lin, Marian Macchi¹, Aditya Raina, Hezi Saar, Jesse Wu, Brian Yang

Winbond Electronics Corporation, San Jose California

¹E-speech Corporation, Princeton, New Jersey

A single-chip solution for text-to-speech synthesis uses analog non-volatile multi-level storage of a corpus of natural speech elements. An embedded micro-controller performs the algorithmic tasks of text-to-speech synthesis. The 80mm² chip fabricated in 0.5μm Flash CMOS operates at 24MHz and 3.0V at 90mW.

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S-P. U

23.1 A 2.5V 57MHz 15-Tap SC Bandpass Interpolating Filter with 320MHz Output Sampling Rate in 0.35 μ m CMOS

Seng-Pan U, R.P. Martins¹, J. E. Franca²

University of Macau, Macau, China, ¹University of Macau and on leave from Instituto Superior Técnico, Lisbon, Portugal, ²Instituto Superior Técnico, Lisbon, and Chipidea Microelectronics, S.A., Portugal

A 57MHz SC bandpass interpolating filter with 320MSample/s output is realized in 0.35 μ m CMOS for DDFS system. 15-tap FIR response is achieved with sampling rate increase and frequency upconversion by translating 22MHz 80MSample/s input to 56MHz 320MSample/s output. Dynamic range is 69dB (1%THD) and 61dB (1%IM3). The filter dissipates 120mW analog and 16mW digital at 2.5V supply.

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J. Hwang

23.2 1W 0.8 μ m BiCMOS Adaptive Q-Current-Controlled Class-AB Power Amplifier for Portable Sound Equipment

Jong-Tae Hwang, Han-Seung Lee

Power Device Division, Fairchild Semiconductor, Puchon, Korea

An AQC class-AB amplifier with low THD and quiescent power consumption uses 0.8 μ m 10V BiCMOS process, occupying 1.8x1.6mm². It has <0.3% THD+N over audio frequency range driving 1W into 8 Ω . It consumes 2.6mA at quiescent condition and has 65.1% power efficiency.

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J. Fattaruso

23.3 Analog Processing Circuits for a 1.1V 270 μ A Mixed-Signal Hearing Aid Chip

**John W. Fattaruso, James R. Hochschild, Walter Sjursen¹, Lieyi Fang,
D. George Gata, Charles M. Branch, Jim Holmes, Zhongnong Jiang,
Shuyou Chen, Kuok Ling, Eugene Petilli², Michael L. Skorcz,
Ricky R. Dickerson, William A. Severin**

Texas Instruments, Dallas, TX, ¹Songbird Hearing, Cranbury, NJ
²Intrinsix, Rochester, NY

A compressing preamplifier, ADC, DAC, output driver and clock oscillator are implemented in a mixed-signal BiCMOS hearing-aid chip with digital filtering. 2.8 μ V input noise floor over the audio band and 0.02% THD are achieved with 270 μ A total battery current.

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A. Tang

23.4 A $3\mu\text{V}$ Offset Operational Amplifier with $20\text{nV}/\sqrt{\text{Hz}}$ Input Noise PSD at DC Employing both Chopping and Autozeroing

Andrew T. K. Tang

Analog Devices, Inc., San Jose, CA

A $3\mu\text{V}$ offset op-amp uses both autozeroing and chopping to give $20\text{nV}/\sqrt{\text{Hz}}$ input noise at DC with low energy at the chopping frequency. The design includes additional circuitry for reduced switching transients. Power consumption is 4mW from a 5V supply. Die area is $0.6 \times 1.12\text{mm}^2$ using a $0.6\mu\text{m}$ double-poly double-metal CMOS process.

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S. Menten

23.5 A $10\mu\text{V}$ -Offset 8kHz Bandwidth 4th-Order Chopped $\Sigma\Delta$ A/D Converter for Battery Management

Peter G. Blanken, Stefan E. J. Menten

Philips Research Laboratories, Eindhoven, The Netherlands

A chopped 4th-order continuous-time 1b $\Sigma\Delta$ A/D Converter with $10\mu\text{V}$ offset and 8kHz bandwidth is for battery current measurement. Chopping at 16kHz, the circuit has a 0.1V input range, a 68dB SNR, and a 1MHz output bit rate. Area is $0.45 \times 0.4\text{mm}^2$ in $0.35\mu\text{m}$ CMOS. Current consumption is $30\mu\text{A}$ at 2.5-4V.

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D. Ma

23.6 A Pseudo-CCM/DCM SIMO Switching Converter with Freewheel Switching

Dongsheng Ma, Wing-Hung Ki, Chi-Ying Tsui

Department of Electrical and Electronic Engineering, The Hong Kong University of
Science and Technology, Hong Kong SAR, China

A single-inductor multiple-output switching converter operates in pseudo-CCM/DCM. It requires freewheeling of the inductor current during the instants when the n switch and all output p switches are off. It is fabricated in a $0.5\mu\text{m}$ CMOS n-well process with $V_{oa} = 2.5\text{V}$ and $V_{ob} = 3.0\text{V}$. With $1\mu\text{H}$ inductor, converter efficiency is 84.7% at 1MHz.

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V. Ceekala

23.7 A Method for Reducing the Effects of Random Mismatch in CMOS Bandgap References

**Vijaya G. Ceekala, Lawrence D. Lewicki, James B. Wieser,
Devnath Varadarajan, Jitendra Mohan**

National Semiconductor Corp., Sunnyvale, CA

A method for reducing the effects of random mismatches in CMOS bandgap references reduces effects of CMOS current-mirror offsets and input-referred offsets of CMOS opamps. The circuit is fabricated in a 0.18 μ m CMOS process. Measured 3 sigma output voltage distribution is ~1%.

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P. Vancorenland

24.1 A Fully-Integrated GPS Receiver Front-End with 40mW Power Consumption

**Michiel Steyaert, Philippe Coppejans, Wouter De Cock,
Paul Leroux, Peter Vancorenland**

Katholieke Universiteit Leuven, Leuven, Belgium

A 0.25 μ m CMOS quadrature complex bandpass low-IF GPS receiver includes an LNA, PLL, mixer and a continuous-time $\Delta\Sigma$ ADC. The chip has -130dBm input sensitivity, 62dB DR, and -32dB IMRR, while consuming 40mW from 2V supply. The chip is 9mm².

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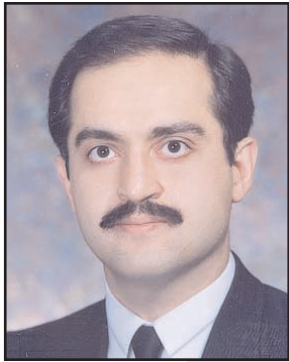


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F. Behbahani

24.2 A 27mW GPS Radio in 0.35 μ m CMOS

**Farbod Behbahani, Hamid Firouzkouhi, Ramesh Chokkalingam,
Siamak Delshadpour, Alireza Kheirkhahi, Mohammad Nariman,
Saket Bhatia, Matteo Conta**

Valence Semiconductor Inc, Irvine, CA

A pure-CMOS 1.575GHz radio integrates a receiver and a synthesizer for GPS application. The receiver path uses a quadrature single-downconversion architecture with an on-chip image reject LPF. It has 4dB NF and -17dBm IIP3 and operates over 2.2V to 3.6V supply and -40 to 85OC. It consumes 27mW from 2.2V supply.

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L. Connell

24.3 A CMOS Broadband Tuner IC

**Larry Connell, Neal Hollenbeck, Mike Bushman, Dan McCarthy,
Steve Bergstedt, Ron Cieslak, Jim Caldwell**

Motorola, Inc., Schaumburg, IL

A single-chip dual-conversion tuner in 0.35 μ m CMOS incorporates both a 50-860MHz LNA and a digital CMOS synthesizer with a -173dBc/Hz phase-noise floor. The synthesizer generates 100mA switching currents at a 12.5MHz rate and all associated in-band spurs are suppressed <0.5 μ Vrms input referred. The 5mm² die consumes 1.5W from a 5V supply.

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T. Umeda

24.4 A 1V 2GHz CMOS Up-Converter using Self-Switching Mixers

Toshiyuki Umeda, Shoji Otaka, Kenji Kojima, Tetsuro Itakura

Toshiba Corporation, Kawasaki, Japan

A 2GHz up-converter uses 0.25 μ m CMOS. Current adding and self-switching mixers are used for 1V operation. A -40dBc LO leakage within a 20mV offset is achieved using a DC offset canceller. The measurement results at 1V supply are 6.7dB conversion gain, 6.5dBm OIP3, \pm 2dB gain deviation from -33 to 75 $^{\circ}$, and 49mW consumption.

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C. Samori

24.5 A CMOS IF Sampling Circuit with Reduced Aliasing for Wireless Applications

Salvatore Levantino*, **Carlo Samori***, **Mihai Banu**,
Jack Glas, **Vito Boccuzzi**

Agere Systems, Murray Hill, NJ, *Politecnico di Milano, Italy
(Agere Systems consultant)

An IF-sampling technique rejects even-order alias channels. A 0.25 μ m CMOS test chip demonstrates 27dB anti-aliasing rejection, 70dB dynamic range, and -121dBm/Hz noise floor, for a 377MHz IF GSM signal, with 52MHz sampling rate.

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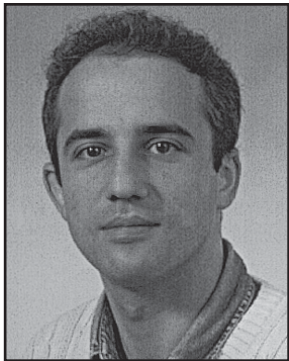


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F. Bruccoleri

24.6 Noise Cancelling in Wideband CMOS LNAs

F. Bruccoleri, E.A.M. Klumperink, B. Nauta

MESA+ Research Institute, University of Twente, Enschede, The Netherlands

A noise-cancelling technique in a wideband LNA achieves low noise figure (NF) and source impedance matching without global feedback. The $0.25\mu\text{m}$ LNA provides $<2.4\text{dB}$ NF from 0.01-2GHz, total voltage gain is 13.7dB, -3dB bandwidth is 0.01-1.6GHz, S_{12} is $<-36\text{dB}$, and S_{11} is $<-10\text{dB}$. IIP2 is 12dBm, and IIP3 is 0dBm drawing 14mA at 2.5V.

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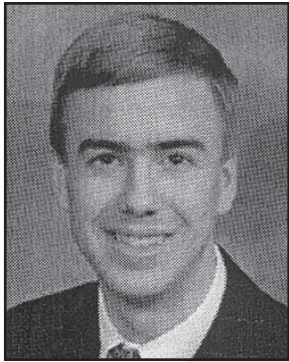


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M. Anders

25.1 A 6.5GHz 130nm Single-Ended Dynamic ALU and Instruction Scheduler Loop

**Mark Anders, Sanu Mathew, Brad Bloechel, Scott Thompson¹,
Ram Krishnamurthy, K. Soumyanath, Shekhar Borkar**

Microprocessor Research Labs

¹Portland Technology Development, Intel Corp., Hillsboro, OR

32b Han-Carlson ALU and 8-entry x 2-ALU instruction scheduler loop for 6.5GHz single-cycle integer execution at 1.2V and 25°C use dual-Vt CMOS technology. A single-ended, leakage-tolerant dynamic scheme enables up to 9-wide ORs with 23% critical path speed improvement, 40% active leakage power reduction compared to Koggie-Stone implementation, dense layout occupying 44,100 μm^2 , and performance scalable to 8GHz at 1.5V, 25°C

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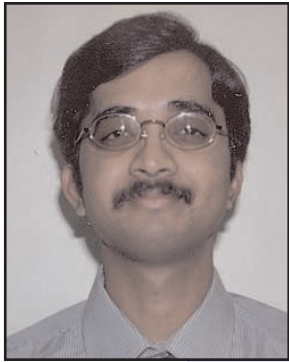


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S. Vangal

25.2 5GHz 32b Integer-Execution Core in 130nm Dual- V_T CMOS

S. Vangal, N. Borkar, E. Seligman, V. Govindarajulu, V. Erraguntla, H. Wilson, A. Pangal, V. Veeramachaneni, M. Anders, J. Tschanz, Y. Ye, D. Somasekhar, B. Bloechel, G. Dermer, R. Krishnamurthy, S. Narendra, M. Stan¹, S. Thompson, V. De, S. Borkar

Intel Corporation, Hillsboro, OR, ¹University of Virginia, Charlottesville, VA

A 32b integer execution core implements 12 instructions. Circuit and body bias techniques together increase the core clock frequency to 5GHz. In a 130nm six-metal dual- V_T CMOS process, the 2.3mm² prototype contains 160k transistors, with RF-ALU units dissipating 515mW at 1.6V.

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R. Rogenmoser

25.3 A 5GHz Dual-Issue Floating-Point Coprocessor with SIMD Architecture and Fast 3D Functions

Robert Rogenmoser, Lief O'Donnell, Steve Nishimoto

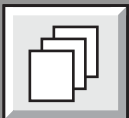
Broadcom, Santa Clara, CA

A floating-point coprocessor, part of a MIPS64 dual-processor SOC, consists of a 32x64b register file and two pipes each with a multiplier, an adder, and a fast 3D approximation unit. It operates up to 1GHz at 1.3W, measures 4.74mm² in 0.13μm CMOS, and has peak performance of 8GFlops per CPU and 16GFlops on the dual-processor SOC.

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N. Tzartzanis

25.4 A 34Word x 64b 10R/6W Write-Through Self-Timed Dual-Supply-Voltage Register File

Nestoras Tzartzanis, William W. Walker, Hoa Nguyen, Atsuki Inoue¹

Fujitsu Laboratories of America, Sunnyvale, CA

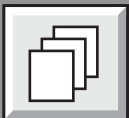
¹Fujitsu Laboratories Ltd., Kawasaki, Japan

A register file leverages from a replica-based control unit to improve reliability, operate in a wide voltage range, and support two supply voltages. The main power supply can be stepped down to reduce power, or shut off for sleep mode. Access time is 1.4ns and power dissipation is 220mW at 500MHz in 1.2V, 0.11 μ m CMOS.

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T. Grutkowski

25.5 The High-Bandwidth 256kB 2nd-Level Cache on an Itanium Microprocessor

Reid Riedlinger¹, Tom Grutkowski²

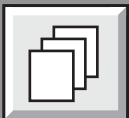
¹Hewlett Packard; Fort Collins, CO, ²Intel; Santa Clara CA

A second-level 256kB unified cache is incorporated into a 1.2GHz next-generation Itanium Microprocessor. The datapath structures provide a non-blocking, out-of-order interface to the processor core achieving a minimum 5-cycle latency with 72GB/s stand-alone bandwidth.

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E. Fetzer

25.6 A Fully-Bypassed 6-Issue Integer Datapath and Register File on an Itanium Microprocessor

Eric S. Fetzer, John T. Orton¹

Hewlett-Packard Company, Fort Collins, CO, ¹Intel Corporation, Santa Clara, CA

A 6-issue integer datapath with a 20-ported 128x65b register file in a 0.18 μ m process operates up to 1.2GHz at 1.5V. Operands bypass through 4 stages, from 34 locations, using $\frac{1}{2}$ clock for execution and $\frac{1}{2}$ clock for bypass. Each result is available for the next instruction.

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J. Tschanz

25.7 Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations on Microprocessor Frequency and Leakage

James Tschanz, James Kao¹, Siva Narendra, Raj Nair, Dimitri Antoniadis¹, Anantha Chandrakasan¹, Vivek De

Microprocessor Research Labs, Intel Corporation, Hillsboro, OR

¹Massachusetts Institute of Technology, Cambridge, MA

Measurements on a 150nm CMOS test chip show that on-chip bidirectional adaptive body biasing compensates effectively for die-to-die parameter variation to meet both frequency and leakage requirements. An enhancement of this technique to correct for within-die variations triples the accepted die count in the highest frequency bin.

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J. Geen

26.1 Single-Chip Surface-Micromachined Integrated Gyroscope with 50°/hour root Allan Variance

John A. Geen, Steven J. Sherman, John F. Chang, Stephen R. Lewis

Analog Devices Inc., Cambridge, MA

A MEMS surface-micromachined gyroscope integrated on a single 3x3mm² chip with a 3μm BiCMOS process has 4μm-thick polysilicon structure, 5V 6mA power supply, 0.05°/√s spot noise, 12.5mV/°/s, >30,000g shock survival, and -55 to 85°C operating range.

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J. Wu

26.2 A Low-Noise Low-Offset Chopper-Stabilized Capacitive-Readout Amplifier for CMOS MEMS Accelerometers

Jiangfeng Wu, Gary K. Fedder, L. Richard Carley

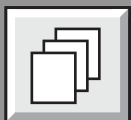
Department of ECE, Carnegie Mellon University, Pittsburgh, PA

A CMOS chopper-stabilized amplifier with both DC and AC offset cancellation, for capacitive readout of motion in MEMS structures, achieves $40\text{nV}/\sqrt{\text{Hz}}$ noise floor, 10mV DC offset, and 40dB sensor offset reduction. The amplifier, integrated into a CMOS-MEMS accelerometer, achieves $50\mu\text{g}/\sqrt{\text{Hz}}$ noise floor.

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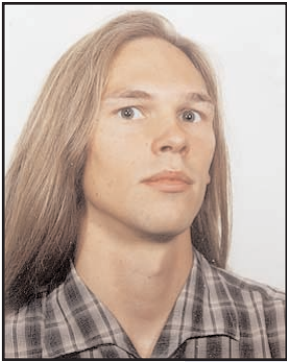


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C. Hagleitner

26.3 A Gas Detection System on a Single CMOS Chip Compromising Capacitive, Calorimetric, and Mass-Sensitive Microsensors

Christoph Hagleitner, Dirk Lange, Nicole Kerness, Andreas Hierlemann, Oliver Brand, Henry Baltes

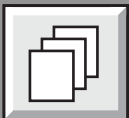
Physical Electronics Laboratory, ETH Zurich, Switzerland

A single-chip chemical microsensor system fabricated in industrial 0.8 μ m CMOS technology includes three different polymer-coated micromachined transducers. The chip forms an integral part of a handheld unit to detect volatile organics. On-chip circuitry includes signal conditioning, A/D-converters, filters, digital controller, and serial bus interface (I²C).

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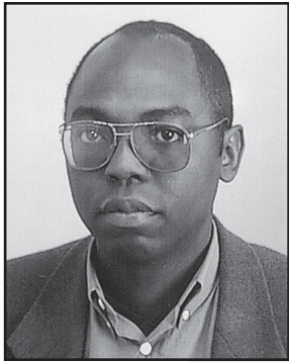


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K. Makinwa

26.4 A Smart CMOS Wind Sensor

Kofi A. A. Makinwa, Johan H. Huijsing

Delft University of Technology, Delft, The Netherlands

A 2-D thermal flow sensor for measurement of wind speed and direction is integrated with interface electronics on a single chip. Three thermal $\Sigma\Delta$ modulators control and digitize the flow-dependent heat distribution in the sensor. Errors in wind speed and direction are $<\pm 3\%$ and $<\pm 2^\circ$ respectively. The 16mm^2 chip uses a standard CMOS process.

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T. Sugiyama

26.5 A 1/4-inch QVGA Color Imaging and 3-D Sensing CMOS Sensor with Analog Frame Memory

**Toshinobu Sugiyama, Shinichi Yoshimura¹,
Ryoji Suzuki, Hirofumi Sumi**

Imaging Device Company, SNC, Sony Corporation, Kanagawa, Japan

¹Sony-Kihara Research Center, Inc., Tokyo, Japan

A 320x240 color imaging CMOS sensor with a current-copier cell array and comparators for column-parallel processing accomplishes video rate depth acquisition. The sensor dissipates 82mW for 3.3kframe/s 3-D sensing with 2.5mm depth resolution, and 36mW for 30frames/s imaging with a single CDS circuit for FPN reduction at 3.3V.

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W. Evans

26.6 An 852x600 Pixel OLED-on-Silicon Color Microdisplay Chip using CMOS Sub-Threshold-Voltage-Scaling Current Driver

Haqing Lin, Eric Naviasky, John Ebner, William Evans, Patrick Farrell, Mike Hufford, Gary Levy, David Wheeler, Bryan Allison, Olivier Prache¹

Tality Analog/Mixed-Signal/RFIC Design Center, Columbia, MD

¹eMagin Corporation, Hopewell Junction, NY

A 16.28x14.2mm² 852x600x3-pixel OLED-on-silicon color microdisplay is implemented in a 0.35 μ m 3.3V/4.0V CMOS process. Using sub-threshold-voltage-scaling, the pixel current is modulated between 250pA and 25nA. The 10M-transistor system supports 15 video modes consuming 200mW for 56.25MHz full-motion video.

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B. Ahuja

26.7 A 30MSample/s 12b 110mW Video Analog Front End for Digital Camera

**Bhupendra K. Ahuja, Eric G. Hoffman, Richard L. Gower,
Charles A. Rogers, J. Antonio Salcedo**

Exar Corporation, Fremont, CA

A highly integrated 30MSample/s video analog front end for >2M pixels camera with 36dB of programmable pixel-by-pixel gain achieves 73dB SNR. Dynamic bias in a 12b pipeline ADC results in 48mW power with 0.4LSB DNL. The die is 7.6mm² in 0.35μm CMOS with 110mW power at 2.7V.

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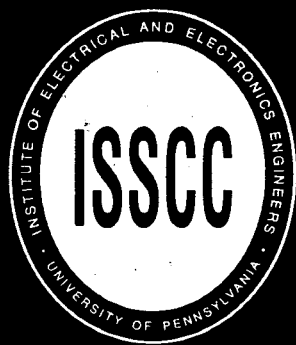
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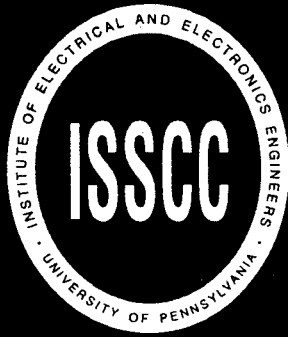
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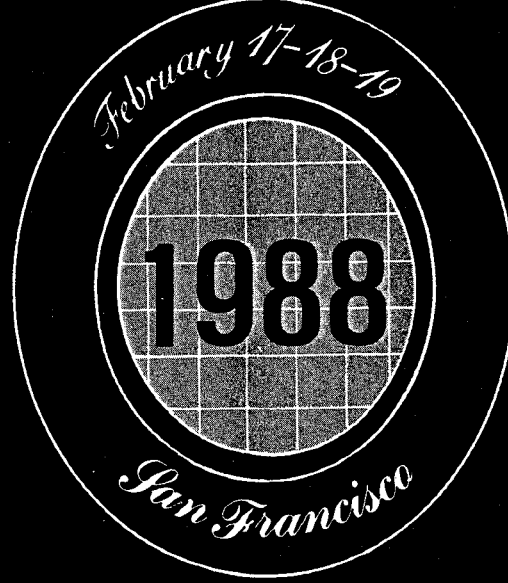
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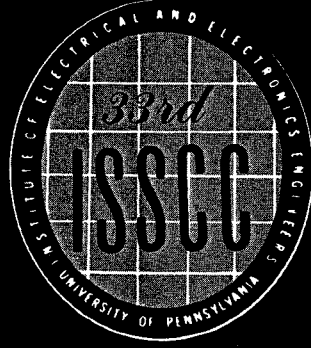
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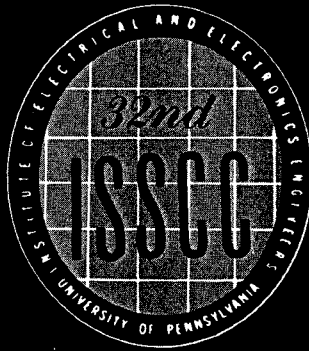
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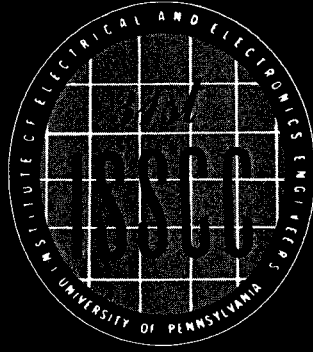
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