2001 DIGEST OF TECHNICAL PAPERS AND VISUALS SUPPLEMENT

ISSCC

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

UNIVERSITY OF PENNSYLVANIA

Welcome

Welcome to the 2001 IEEE International Solid-State Circuits Conference on CD-ROM!

This CD is designed so that you may locate technical papers and corresponding presentation Visuals by session or by author, as well as with full-text search.

Technical papers and visuals were originated, generally, as electronic files; all materials were converted to Adobe Acrobat PDF format for cross-platform access. Since, in a very few cases, some of the materials were scanned, and since the figures and Visuals originated with the authors, the viewing quality will vary with the size and quality of fonts used. Generally speaking, even though the viewing quality on your monitor may vary, all papers print clearly. Note that the technical papers are fully edited prior to publication in the Digest, but that Digest figures and Visuals are as received from the authors.

Thank you and Enjoy!

Laura Chizuko Fujino
ISSCC Director of Publications/Presentations
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INTRODUCTION

This Electronic Guide file contains hypertext links within the Guide and to separate paper files. Links are represented by colored text (e.g. a name or title); clicking on the text activates the link.

Before you start browsing and using the information on this CD-ROM, you will need to install Adobe Acrobat Reader 4.0. If you already have Acrobat Reader installed on your system, make sure it is version 4.0 or higher and includes the Search plug-in.

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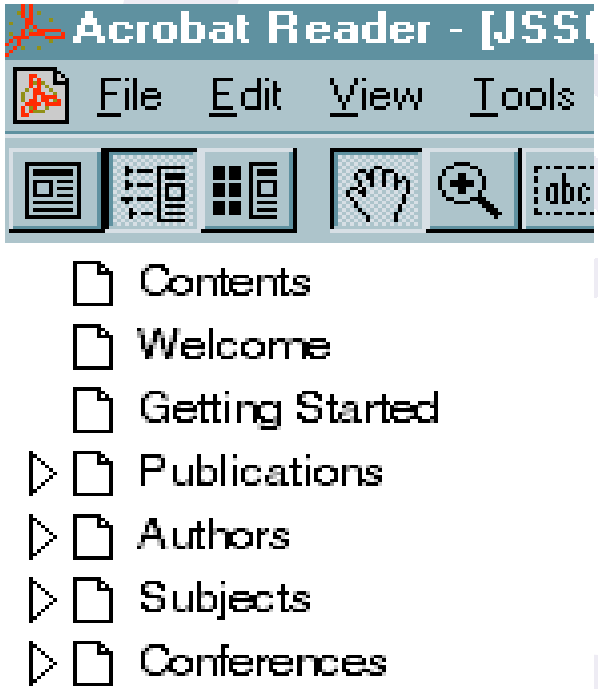

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NAVIGATION BUTTONS

This Guide contains a variety of navigational aids to help you easily explore the contents.

Section Map

The Electronic Guide is constructed in sections: e.g. Papers, Authors, Getting Started. The current section is shown at the top of each page. The "path" to this section is shown at the right. Clicking these text buttons moves you to the start of that section.

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Click to advance to the next page in the section.

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The Page Up and Page Down keys perform the same functions.

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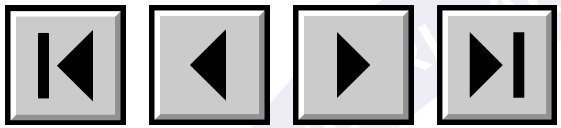

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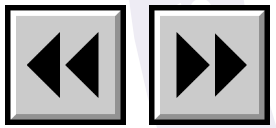

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SEARCHING

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Typing a term in the text box at the top of the Search dialog box and pressing the “Search” button causes a full-text search of all words in the body of papers in the collection.

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Foreword

The Internet Age: Technologies Driving Digital Convergence

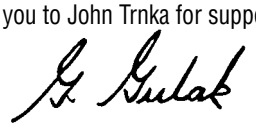
Welcome to the 48th annual ISSCC. ISSCC 2001 promises to be an exciting one and continues ISSCC's proud tradition as the foremost global forum for presentation of advances in solid-state circuits. ISSCC 2001 consists of 165 technical papers in 25 Sessions, a three-paper Plenary Session, eight evening panels, six tutorials, a short course, and a workshop. The international scope of the conference is reflected in the geographical origin of the paper submissions. This year, 53% of the accepted papers are from North America, 21% from Europe, and 26% from the Far East. Of these papers, 70% are from industry and 30% are from universities and/or industry-university collaborations.

The Internet Age is characterized by a convergence of communications and computing technologies that will undoubtedly change how we live and work. The rapid growth and development of the internet has been largely driven by advances in integrated circuits, and thus THE INTERNET AGE: TECHNOLOGIES DRIVING DIGITAL CONVERGENCE is a timely theme for ISSCC 2001. The technical infrastructure required to support the internet is broad, and includes technologies and circuits related to all types of networks, both local and wide-area, wired and wireless as well as general-purpose microprocessors, memory systems and application-specific signal processors for data, voice and image processing applications. Papers spanning the latest analog, digital, and mixed-signal circuit innovations in each of these areas are included in the technical paper presentations of this year's conference. In addition, the three Plenary session papers, the short course and tutorials are tightly coupled to the theme.

The quality of this year's technical papers is extremely high, continuing the tradition of excellence long associated with the ISSCC. In the microprocessor area, for instance, there are benchmark papers in Sessions 15 and 20 describing GHz microprocessors. High-speed digital interfaces are rapidly evolving and the latest developments are presented in Session 4. On the topic of memories, paper Session 24, describes the design of a 4Gb DDR SDRAM. Session 2 describes innovations in non-volatile memory and presents a 1Gb flash memory. In the area of signal-processing systems, a 90mW MPEG-4 video codec is presented in Session 9; a complete set-top box system-on-chip, an ultra-low-power cryptography processor, and some of the first chips to support the 54Mb/s IEEE 802.11a WLAN standard are presented in Session 21. In the wireless area, Session 13 presents several fully-integrated Bluetooth transceivers and a fully-integrated 5GHz wireless LAN receiver in CMOS. In the wireline area, important developments in the design of analog front ends for xDSL and 1000Base-T systems are presented in Session 19. Analog circuit advancements in the area of ADCs are presented in Session 8 with two papers describing 6b ADCs that operate in excess of 1GSample/s. Many CMOS image sensors with embedded processors are described in Session 6. Advanced technologies such as biological integrated circuits, molecular electronic devices, and magnetoresistive RAMs can be found in Session 7. These are just a select few of my favorite sessions and milestone papers; undoubtedly, you will discover more of your own.

Many people have contributed to the success of ISSCC 2001. The US, Far East, European and Executive Committees are composed of 163 experts who met in April, June, August, September, and October to plan the conference. I express gratitude and appreciation to all of them. In particular, I thank Watanabe-san the Far East Chair, Arai-san the Far East Secretary, Yamashina-san the Far East Assistant Secretary, Rudy Van de Plassche the European Chair, and Jan Sevenhans the European Secretary, for their leadership, assistance and support. I would also like to thank the Subcommittee Chairs for their tremendous efforts: Behzad Razavi (Analog), Ian Young (Digital), Dennis Polla (Imagers, Displays & MEMS), Bruce Bateman (Memory), Anantha Chandrakasan (Signal Processing), John Cressler (Technology Directions), Bob Bayruns (Wireless Communications), and Russ Apfel (Wireline Communications). Their leadership and the efforts of their subcommittees have resulted in a quality conference again this year. I express deep appreciation to all members of the ISSCC Program Committee for the tremendous commitment of time and expertise. I also thank all of the authors and speakers for contributions in making this year's conference well worth attending.

Additionally, I express thanks to Willy Sansen for valuable assistance as Vice-Chair; to Diane Suiters and her colleagues at Courtesy Associates for Conference arrangements, operations, registration, and valuable assistance; the staff at MiraCD for their assistance in helping us migrate to a new electronic submission format; John Wuorinen for his editorial skills; Steve Bonney of Letter Systems for his efforts in helping to produce the Advance Program and Digest; Laura Fujino and Ken Smith for their extensive work with the Press Kit, press conferences, awards, CD-ROM and slide supplement; to Frank Hewlett for his superb efforts in keeping track of action items and Web operations; and a special thank-you to John Trnka for support, guidance and leadership. I know you will find this year's conference informative, enjoyable, and rewarding!



Glenn Gulak, ISSCC 2001 Program Chair

Session 6
CMOS Image Sensors with Embedded Processors

Evening Sessions
Discussion Sessions

Session 7
Technology Directions: Advanced Technologies

Session 8
Nyquist ADCs

Session 9
Integrated Multimedia Processors

Session 10
Wireless Building Blocks I

Session 11
SRAM

Session 12
Signal Processing for Storage and Coding

Session 13
Wireless LAN

Session 14
Gigabit Optical Communications II

Session 23
Analog Techniques

Session 24
DRAM

Session 25
Clock Generation and Distribution

Session 26
Wireless Building Blocks II

Short Course

CMOS RF CIRCUITS

This Short Course is intended to jumpstart engineers in design and development of CMOS circuits for wireless applications. Course completion provides an overall perspective of system tradeoffs along with detailed circuit design strategies for key RF wireless transceiver building blocks. Topics include overview of mobile wireless systems and key metrics of RF design, low noise amplifier characteristics, tradeoffs and designs, fundamentals of mixer design for RF receivers, and CMOS oscillator circuit analysis and design.

OUTLINE

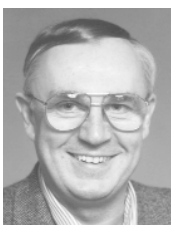
MOBILE TRANSCEIVER DESIGN SYSTEM OVERVIEW

RF designers must consider noise figure, intercept, and compression points in the context of system requirements such as sensitivity, selectivity, and resilience to blocking and interference. Significance of power consumption in modern mobile communications and trade-off among cost, power, size, and weight of mobile terminals in CMOS implementations are discussed.

Instructor: Qiuting Huang received PhD from Katholieke Universiteit Leuven (1987). After five years as lecturer at the University of East Anglia, Norwich, UK, he joined the Integrated Systems Laboratory, Swiss Federal Institute of Technology (ETH), Zurich. His research interests are in the design of radio-frequency and baseband ICs for wireless communications. He is member of the ISSCC and European Solid-State Circuit Conference Program Committees. He was awarded the Transactions on Electronics best paper award (1997) and participated in the ISSCC Best Panel.

LOW-NOISE AMPLIFIERS

Design issues for RF low-noise amplifiers in fine-line CMOS and basic LNA performance parameters are reviewed. Gain, frequency, noise, linearity, power dissipation, supply voltage, and input/output matching tradeoffs are presented in terms of CMOS scaling trends for active and passive devices in single-ended and fully-differential implementations. Merged LNA/filter topologies with design examples illustrating tradeoffs are discussed.



Instructor: David J. Allstot received PhD from UC Berkeley in 1979. He is currently the Boeing-Egtvedt Chair Professor in EE at the University of Washington and a Technical Consultant with Mobilian Corp. He has advised about 60MS and PhD graduates, published more than 150 papers, and received several best paper awards and several outstanding teaching and advising awards. His current research includes data converters and RF circuits. He is an IEEE Fellow.

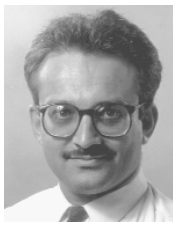
CMOS UP AND DOWN CONVERTERS

Modern transceivers often use co-designed receiver architectures and mixer topologies. For these architectures, different up and down converter CMOS circuits are discussed in detail. The realization of quadrature and image-rejection mixers in combination with poly-phase filters is presented. Relevant design examples and limitations of CMOS transceiver are reviewed.

Instructor: Michiel S.J. Steyaert received PhD from Katholieke Universiteit Leuven, Heverlee, Belgium in 1987. He joined the K.U. Leuven Laboratory ESAT in 1983 where he is Professor. His current research interests are high-performance and high-frequency analog integrated circuits for telecommunication systems. He received the European Solid-State Circuits Conference Best Paper Award (1990), the ISSCC Evening Session Award (1995, 1997), the 1999 IEEE Circuit and Systems Society Guillemin-Cauer Award and the 1991 NFWO Alcatel-Bell-Telephone award for innovative work in integrated circuits for telecommunications.

FUNDAMENTAL ASPECTS OF OSCILLATOR DESIGN

Oscillators have traditionally lagged amplifiers in terms of well-formed intuitions that enable the circuit designer to arrive at the optimum solution. Simple, accurate, yet physical understanding of noise and large-signal operation enables complete understanding of oscillators, and points the way to state-of-the-art solutions. These concepts are illustrated on frequently-used RF-CMOS oscillators.



Instructor: Asad A. Abidi received PhD from U.C. Berkeley in 1981. He worked at Bell Labs, Murray Hill, NJ until 1985 when he joined UCLA where he is Professor. He served as Editor of the IEEE Journal of Solid-State Circuits (1992-1995). He received the TRW Award for Innovative Teaching (1988) and the IEEE Donald G. Fink Award (1997), and is co-recipient of the Best Paper Award at the European Solid-State Circuits Conference (1995), the ISSCC Jack Kilby Best Student Paper Award (1997), the ISSCC Jack Raper Award for Outstanding Technology Directions Paper (1997), the Design Automation Conference Design Contest Award (1998), and an IEEE Millennium Medal. He is an IEEE Fellow.

Tutorials

Front-End Circuits for Optical Communications

An introduction to optical receiver circuits is presented with focus on integration at >10Gb/s data rate in SiGe technology. Basic system requirements and design considerations. TZ-, AGC and limiting amplifiers, clock and data recovery, demultiplexer circuits, linear binary clock recovery architectures, and SONET jitter characteristics will be discussed.

Instructor: Yuriy M.Greshishchev, Nortel Networks, Ottawa, Canada received the PhD in Electrical and Computer Engineering from V.M. Glushkov Institute of Cybernetics, Microelectronics Division, Kiev, Ukraine, in 1984. He is an advisor on high-speed communications circuit design developing highly integrated circuits in emerging technologies for 10-40Gb/s optical communications. His recent work is on a 10Gb/s fully-integrated SiGe receiver for SONET. He has co-authored 2 books and numerous technical papers on high-speed communication circuit design and data converters.

Logical Effort - Designing Fast CMOS Circuits

Designers of high-speed integrated circuits face a bewildering array of choices and too often spend frustrating days tweaking gates to meet speed targets. Logical Effort provides a simple method for estimating gate delays and evaluating tradeoffs of circuit topologies and gate sizes.

Instructor: David Harris is Assistant Professor of Engineering at Harvey Mudd College. His research interests are in the area of high-speed integrated circuit design, especially timing, domino circuits, and arithmetic units. He is coauthor of a book on Logical Effort and author of Skew-Tolerant Circuit Design. Prof. Harris has consulted for numerous design teams at Sun Microsystems, Hewlett-Packard, Intel, and elsewhere in the area of high speed circuits. He received M.Eng. and SB from MIT in 1994 and PhD in EE form Stanford University In 1999 and M.Eng. and S.B. from MIT in 1994.

Network Processing ICs

Architectural and design issues of the ASIC architectures dedicated to specific network processing functions, known as packet processors, for key functions in high-speed switches and routers will be reviewed. Topics include: (1) Switch architecture and queue management: Ethernet switch architectures, input queuing vs. output queuing, multicasting, QoS, buffer management (2) Multi-layer switching: L2 search and learn, VLAN, L3 longest-prefix-match search, IP multicast, L4-7 classification (3) Emerging standards/interfaces: 10G Ethernet (XGMII), UTOPIA-4, Packet-over-SONET (POS), Common Switch Interface Specification (CSIX), InfiniBand

Instructor: C. Bernard Shung, Allayer Communications, San Jose, CA received PhD in EECS from UC Berkeley in 1988. He is Design Manager responsible for highly-integrated multi-layer products. He led the first 10GbE switching processor with 44Gb/s bandwidth. He has been at IBM Almaden, CA and Qualcom, San Diego, and was Professor of EE at National Chiao Tung University, Hsinchu, Taiwan, where his research was on ATM switching, wireless communications, error-correcting codes, and cryptography.

Low-Power Design Techniques for Microprocessors

Microprocessors have become prevalent in today's handheld wireless electronic era. The design of the microprocessor significantly impacts power consumption and hence battery life, a crucial metric in any portable device. This tutorial discusses design techniques and issues for low power microprocessor design. The presentation covers design, from system architecture to transistor sizing. Areas covered include static and dynamic power consumption, process issues, leakage control, logic design styles and transistor sizing.

Instructor: Simon Segars, ARM Inc., Austin, TX holds a BEng in EE from Univ. of Sussex, England, and a MSc in Low-Power CPU Design from Univ. of Manchester, England. He is Director of CPU Development at ARM Austin Design Center. At ARM since early 1991, he has worked on most fo ARMs CPU products since then. He led development of the ARM7 and ARM9 Thumb families now oversees architectural specification of future high-performance processors. He holds a number of patents on embedded CPU architectures.

Broadband Design for Wireless and Wired Systems

System requirements and IC design techniques for broadband wireless and wired systems are discussed. Two example systems, high-definition television and cable modems, are used as real-world examples. Broadband design issues are contrasted with the narrowband design styles that are well known to wireless engineers today. In particular, design techniques for realizing wide bandwidth matching, low noise, and low distortion including composite beats are described in detail.

Instructor: Bud Taddiken, Microtune, Plano, TX joined Microtune in 1996 as Director of RFIC Development and became Vice President of IC Engineering in 1998. From 1983 to 1996, he held various positions with Texas Instruments, most recently RFIC Design Manager for Transmitters and PLLs and Member, Group Technical Staff. He has authored or coauthored over 30 conference or journal papers and holds a BSEE from MIT and six US patents.

Integrated Electronics for Displays

Displays are the primary interface for information technology users, especially in today's Internet age. Today's displays must compete in a cost-sensitive market, which drives innovation in display module technology, its interface and timing control components, and system integration. An overview of the latest display technology includes coverage of key electronic components used today and future opportunities for integration.

Photo Not Available

Instructors: Philip Alvelda, MicroDisplay, San Pablo, CA received BS in Physics and Computer Science at Cornell University in 1986, and MS and PhD in Electrical Engineering and Computer Science from MIT in 1993 and 1994. After working at NASA developing high-precision CCD star and target trackers, he founded and was Chief Technology Officer of the MicroDisplay Corp. He has been a Principal Investigator and director of several DARPA research projects in display technology. He is currently CEO of Idetic, Inc., a member of IEEE and SID, and is an invited industry speaker. He holds 15 patents and has presented more than 30 technical papers.

Instructors: Kai Schleupen, IBM, Yorktown Heights, NY Dr. Schleupen received MS in 1989 and PhD in 1995, at the Laboratory for Flat Panel Displays of University of Stuttgart, Germany. From 1995 to 1996 he worked in the Display Research Dept at AT&T Bell Labs, Murray Hill, NJ. In 1996, he joined the IBM T.J. Watson Research Center in Yorktown Heights, NY, where he now manages the Display Design and Electronics Dept. responsible for design of high-resolution direct-view displays for desktop and portable applications. He holds 12 patents and is author or co-author of over 20 technical publications. He is member of IEEE and SID.

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* Committee Representative on Technology Directions Subcommittee

ISSCC 2002 Call for Papers

Monday - Wednesday, February 4 - 6, 2002
San Francisco Marriott Hotel, San Francisco, CA

Original Papers are Solicited in Subject Areas Including but not Limited to the Following:

ANALOG --- amplifiers; dc-dc converters; continuous-time & discrete-time filters; comparators; multipliers; voltage references; sample-and-hold circuits; Nyquist-rate & oversampling A/D and D/A converters; power-control circuits; consumer electronics; non-linear analog circuits, opamps, switched-capacitor circuits, oscillators.

WIRELESS & RF COMMUNICATIONS --- transceiver circuits and subcircuits for RF/IF/baseband; frequency synthesis; phase-locked loops, wireless local-area networks, GSM/EDGE/CDMA/3G, active antennas, DVB, cellular/PCS RF front-end circuits; HDTV, Satellite TV, MMDS.

WIRELINE COMMUNICATIONS --- LAN; WAN; FDDI; Ethernet; token ring; Fiber Channel, SONET; ATM; ISDN; xDSL; optical data links, power-line/phone-line home networks; subscriber-line circuits, modems.

DIGITAL --- design, fabrication and test of digital LSI and VLSI systems; microprocessors and coprocessors; I/O and interchip communication; fixed and reconfigurable logic arrays; clocking; high-performance and low-power logic micro-architecture and transistor circuit techniques.

IMAGERS, DISPLAYS, & MEMS --- image sensors and related imaging techniques; smart sensors; integrated sensors and transducers; display drivers and controllers; thin-film-transistor interface circuits; flat-panel and projection displays; sensor interface circuits.

MEMORY --- design, fabrication, and test of static and dynamic memories; memory architecture; redundancy and self-test; nonvolatile and read-only memory; special-purpose memories; embedded memories; memory systems.

SIGNAL PROCESSING --- digital & analog signal processors; graphic processors; magnetic-media circuits; HDTV; image and voice-band processing and compression circuits; multimedia/telecom digital signal processors and cores; encryption processors; system-on-a-chip design methodologies.

TECHNOLOGY DIRECTIONS --- advanced circuit technologies and techniques: SiGe, SOI, deep submicron, compound semiconductor; superconductivity, photonics, ferroelectrics, nanoelectronics, 3D-electronics and technologies for bio-medical and microfluidic applications; low-power low-voltage analog and digital, mixed analog-digital, high-speed, RF, on-chip passive RF components; microprocessor architectures, analog processors and memories, optical processors and backplanes, neural processors, fuzzy logic, multi-valued logic.

A submission may be accepted as either a regular paper or a short paper. A regular paper is allowed 23 minutes for presentation and 7 minutes for questions. Short papers are allowed 15 minutes total for both presentation and questions. Regular and short papers have the same submission requirements and the same quality standards. They differ only in the determination by the Program Committee of the time required to present the key ideas. Companion papers for large chips that require two paper slots to discuss both architecture and circuit details are encouraged.

***** 2002 Conference Theme *****

ICs for Information Technologies

Submission Deadline is Wednesday, September 5, 2001

Authors must go to **http://www.sscs.org/isscc/submit** prior to submitting a paper to obtain a submission number and to complete the information for the Advance Program. This WEB site will be operational on July 1, 2001. For details, please refer to the complete Call for Papers available in April from the ISSCC Web site at **http://www.sscs.org/isscc/2002/cfp.htm.**

Sunday, February 4th — **ISSCC 2001 TUTORIALS**

8:00 AM	Front-end Circuits for Optical Communications/Logical Effort-Designing Fast CMOS Circuits/Network Processing ICs/Low-Power Design Techniques for Microprocessors/Broadband Design for Wireless and Wired Systems/Integrated Electronics for Displays

SSCTC WORKSHOP

8:00 AM	Workshop on RF Circuits for 2.5G and 3G Wireless Systems (For Experts)

Monday, February 5th — **ISSCC 2001 PAPER SESSIONS**

8:30 AM	Session 1: Plenary Session (Salons 7-9)				
1:30 PM	Session 2: Non Volatile Memory (Salon 1-6)	Session 3: Oversampling Converters (Salon 7)	Session 4: High Speed Digital Interfaces (Salon 8)	Session 5: Gigabit Optical Communications I (Salon 9)	Session 6: CMOS Image Sensors with Embedded Processors (Salon 10-15)
5:00 PM	Author Interviews (Far End of Grand Assembly) and Social Hour (Golden Gate B and Foyer)				

ISSCC 2001 DISCUSSION SESSIONS

8:00 PM	E1: Does Fabless mean Futureless for Imaging? (Salon 1-6)	E2: 10 Years of RF-CMOS - But How Many Products Today? (Salon 7)	E3: Has Scaling Created a Microprocessor Monster? (Salon 8)	E4: How Will Future Portable Systems Store and Access Data? (Salon 9)

Tuesday, February 6th — **ISSCC 2001 PAPER SESSIONS**

8:30 AM	Session 7: TD: Advanced Technologies (Salon 1-6)	Session 8: Nyquist ADCs (Salon 7)	Session 9: Integrated Multimedia Processors (Salon 8)	Session 10: Wireless Building Blocks I (Salon 9)	Session 11: SRAM (Salon 10-15)
1:30 PM	Session 12: Signal Processing for Storage and Coding (Salon 1-6)	Session 13: Wireless LAN (Salon 7)	Session 14: Gigabit Optical Communications II (Salon 8)	Session 15: Microprocessors (Salon 9)	Session 16: Integrated MEMS and Display Drivers (Salon 10-15)
5:15 PM	Author Interviews (Far End of Grand Assembly)				

ISSCC 2001 DISCUSSION SESSIONS

8:00 PM	E5: Embedded DRAM (Salon 1-6)	E6: Broadband Access (Salon 7)	E7: 100Cubed: Science or Fiction? (Salon 8)	E8: Are Startups Killing Innovation? (Salon 9)

Wednesday, February 7th — **ISSCC 2001 PAPER SESSIONS**

8:30 AM	Session 17: TD: 3D Technologies and Measurement Techniques (Salon 1-6)	Session 18: 3G Wireless (Salon 7)	Session 19: Voiceband, xDSL and Gigabit Ethernet Circuits and Transceivers (Salon 8)	Session 20: Multi-GigaHz Microprocessor Technologies (Salon 9)	Session 21: Signal Processing for Communications (Salon 10-15)
1:30 PM	Session 22: TD: System - On-A-Chip (Salon 1-6)	Session 23: Analog Techniques (Salon 7)	Session 24: DRAM (Salon 8)	Session 25: Clock Generation and Distribution (Salon 9)	Session 26: Wireless Building Blocks II (Salon 10-15)
5:15 PM	Author Interviews (Ballroom Foyer South)				

Thursday, February 8th — **ISSCC 2001 SHORT COURSE**

8:00 AM	CMOS RF Circuits (Sessions at 8:00 AM, 10:00 AM, and 1:30 PM)

ISSCC 2001 MICROPROCESSOR WORKSHOP

8:00 AM	Microprocessor Design

RECAPITULATIONS

This, the year-2001 edition of the ISSCC Visuals Supplement (formerly called the Slide Supplement), marks the twelfth appearance of this novel product in conference documentation. It was first provided at ISSCC90, eleven years ago, following a conceptualization process begun only a few months earlier.

The acceptance of the first edition was sufficiently strong that we were encouraged to continue the logical development of the original concept. The result is open before you now. This year, again, it has been provided to every full registrant at ISSCC as part of their registration package, with world-wide delivery by priority or global mail, for expected arrival within three weeks of the end of the Conference.

While the basic idea remains the same – to provide a record of what was actually presented at ISSCC, very shortly after the close of the Conference, the mechanisms have varied in detail over the years. This year, the experiment in electronic projection introduced in three sessions last year, was extended to all 168 papers of the Conference.

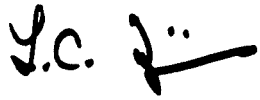
To facilitate this process, all speakers were requested to send hard and soft copies of their presentation a week before the Conference. For Speaker Rehearsal, each presentation was converted from the received format to PDF to ensure consistency and quality. The paper copies provided were used to check for aberrances in the code-conversion process, and to facilitate communication of the changes inevitably required by some speakers. Generally speaking, the process of conversion went smoothly, although some difficulty was encountered with presentations initiated in Framemaker and Latex. For the majority, which were originated in Powerpoint, very little difficulty was found.

In the checking process introduced this year, each speaker was given a CD containing the presentation, for initial review and verification at Speaker Rehearsal. Then, following last-minute changes initiated by the speaker, a full-session PDF version was loaded on CD-ROM for back-up. The actual presentation was run from hard disc on two laptops, each driving a separate display, one system providing the back up for the other. As a result of the more-integrated process made possible by electronic projection, the quality of both the presentation visuals and the Visuals-Supplement pages has improved from past years.

Of course, all of this virtually real-time process was possible only through the heroic cooperation of many many people: First and foremost, I must acknowledge the authors and speakers, who, almost without exception, graciously provided the requested hard-copy and soft-copy materials in a timely and effective fashion. Moreover, as a glimpse of the following pages will attest, the quality provided generally ranged from good to better than excellent. By and large, guidelines concerning line thickness, information density, and the like, were closely followed. As well, the electronic-processing procedure for book production introduced three years ago, but extended this year, continued to sustain a noteworthy quality improvement in this final product.

Overall, a great deal of detailed work was necessary by a large number of volunteers, styled “The Saratoga Group” in recognition of the hotel meeting room in which the original Supplement was assembled. Each of these individuals, in a very special way, is deserving of our appreciation: To Steve Bonney, David Cassan, Tooraj Esmailian, Ted Fill, Warren Gross, Steve Hranilovic, Agustin Lebron, Shahriar Mirabbasi, Kostas Pagiamtzis, Jennifer Rodrigues, Saman Sadr, Kenneth Smith, Marcus van Ierssel, and Laurie Wood, must go our heartfelt appreciation for a job well and truly done, a job which occupied many of them virtually every waking hour for the best part of a week, and others for even more!

Finally, we wish to acknowledge the outstanding contribution of Richard Simmonds and his willing staff at the Business Center of the San Francisco Marriott Hotel. Many thanks to you all!



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Volume MMI
Visuals Supplement

Editor: Laura Chizuko Fujino

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0-7803-6608-5

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Clock Generation and Distribution

Session 26
Wireless Building Blocks II

Conference Information

IEEE International Solid-State Circuits Conference

The Beatrice Winner Award

2001

Jafar Savoj

Behzad Razavi

for EDITORIAL EXCELLENCE in the paper

A 10Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection

IEEE International Solid-State Circuits Conference

ISSCC

The Lewis Winner Award 2000


Thomas Burd


Trevor Pering


Anthony Stratakos


Robert Brodersen

for the OUTSTANDING PAPER

A Dynamic Voltage Scaled Microprocessor System

IEEE International Solid-State Circuits Conference

ISSCC

The Jack Raper Award

2000

Roy Scheuerlein

William Gallagher

Stuart Parkin

Changchuan Lee

Samuel Ray

Raphael Robertazzi

William Reohr

for the OUTSTANDING TECHNOLOGY-DIRECTIONS PAPER

A 10ns Read and Write Non-Volatile Memory Array Using a Magnetic Tunnel Junction and FET Switch in each Cell

IEEE International Solid-State Circuits Conference

ISSCC

The Jack Kilby Award

2000

James Maligeorgos

John Long

for the OUTSTANDING STUDENT PAPER

A 2V 5.1-5.8GHz Image-Reject Receiver with Wide Dynamic Range

IEEE International Solid-State Circuits Conference

ISSCC

The Jack Kilby Award

2000

Arne Buck

Charles McDonald

Stephen Lewis

T.R. Viswanathan

for the OUTSTANDING STUDENT PAPER

A CMOS Bandgap Reference without Resistors

IEEE International Solid-State Circuits Conference

ISSCC

Evening-Session Award

2000

Todd Brooks
Organizer

Theo Claasen

Nicky Lu

Behzad Razavi

Nav Sooch

T.R. Viswanathan

Bob Wiederhold

David Robertson
Moderator

for the OUTSTANDING PANEL

Engineering Resources: Train, Buy, Rent or Steal?

IEEE Journal of Solid-State Circuits

Best Paper Award

1999

Brian Brandt

Joseph Lutsky

for the PAPER

A 75mW 10b 20MSPS CMOS Subranging ADC with 9.5 Effective Bits of Nygquist

IEEE Solid-State Circuits Society

Outstanding Chapter Award 2000

Hajimi Ishikawa
Chapter Chair

Hidetoshi Onodera
Treasurer

Hajime Ishikawa
Chair

Toshiaki Masuhara
AdCom

Takeshi Imamura
Secretary

Japan Chapter

IEEE Solid-State Circuits Society

Pre-Doctoral Fellowship

2000
2001

Liang Dai

at the University of Minnesota

IEEE Solid-State Circuits Society

Pre-Doctoral Fellowship

2000
2001

Jafar Savoj

at the University of California, Los Angeles

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

W.R.G. Baker Prize Paper Award 2000

Keshab Parhi

for the OUTSTANDING PAPER

Low-Energy CSMT Carry Generators and Binary Adders

Institute of Electrical and Electronics Engineers

Fellow Award

2001

John J. Corcoran

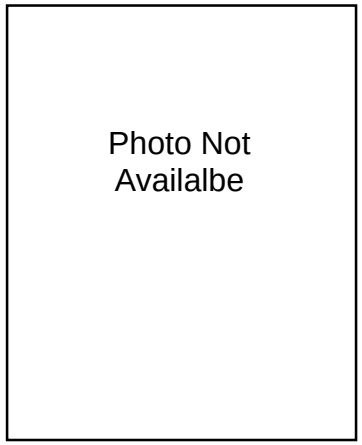
for CONTRIBUTIONS to

high-performance analog-to-digital converters.

Institute of Electrical and Electronics Engineers

Fellow Award

2001



Sang H. Dhong

for CONTRIBUTIONS to

high speed processor and memory chip design.

Institute of Electrical and Electronics Engineers

Fellow Award

2001

Yoshiaki Daimon Hagiwara

for PIONEERING WORK

on, and development of, solid-state imagers.

Institute of Electrical and Electronics Engineers

Fellow Award

2001

Masao Hotta

for CONTRIBUTIONS to

the development of low-power video-frequency analog-to-digital converters for mixed-signal system Large-Scale Integrated circuits.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

Fellow Award

2001

Paul James Hurst

for CONTRIBUTIONS to

the design of CMOS integrated circuits for telecommunications and magnetic recording.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

Fellow Award

2001

Wei Hwang

for CONTRIBUTIONS to

high-density cell technology and high-speed Dynamic-Random-Access-Memory design.

Institute of Electrical and Electronics Engineers

Fellow Award

2001

David Andrew Johns

for CONTRIBUTIONS to

the theory and design of analog adaptive integrated circuits used in digital communications.

Institute of Electrical and Electronics Engineers

Fellow Award

2001

Stephen H. Lewis

for CONTRIBUTIONS to

the development of pipelined analog-to-digital converters.

Institute of Electrical and Electronics Engineers

Fellow Award

2001

Peter W. Verhofstadt

for sustained LEADERSHIP and CONTRIBUTIONS to

microelectronics research and development.

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- 1.2 Broadband Access: the Last Mile
- 1.3 Microprocessors for the New Millennium – Challenges, Opportunities and New Frontiers

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- 4.6 Digitally-Controlled DLL and I/O Circuits for 500Mb/s/pin x16 DDR SDRAM
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Paper Abstracts

K. Enoki

1.1: i-mode: 21st Century Mobile Internet

Kei-ichi Enoki

NTT DoCoMo, Tokyo, Japan

Mobile telephone services in Japan are expanding rapidly. The number of users exceeds 60M, surpassing the number of fixed phone subscribers. In this market, much attention has been focused on “i-mode.” i-mode has commanded an increasing number of subscribers since service began, 2/22/99, reaching 12M subscribers in 18 months. i-mode mobile phones feature browsers that read HTML, and send and receive e-mail or obtain information off of the Web. i-mode offers information on 1,100 portal sites from 600 companies, with contents covering: airline and concert tickets, book and CD sales, downloads of games, animations, and ringer tones, horoscopes, restaurant guides, news and weather forecasts, and banking and trading. There are already >23k independent Web sites accessible by inputting URL address, and >200 search engines. In the future, i-mode will feature Java technology and Secure Socket Layer (SSL) functions, and in the era of IMT2000 (3rd Generation), image transmission will become a reality.

The i-mode will change how things are done and assist in creating new industries, not only in mobile communications, but also in many other businesses. It will be at the core of an IT revolution as a Mobile Internet Platform, and contribute to constructing a more affluent society.

Progress in IC technologies will have a significant effect on i-mode evolution. The key to i-mode evolution is processors that handle audio signals and execute a variety of applications. This paper discusses the current status and future of i-mode services, and IC and other component technologies in the context of these services.

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L. Cloetens

1.2: Broadband Access: the Last Mile

Leon Cloetens

Alcatel Microelectronics, Zavantem, Belgium

Driven by deregulation, a multitude of new transmission technologies have been deployed and standardized in recent years.

The classical plain old telephony service (POTS) network is reused for DSL applications. Optical fiber is increasingly deployed in new networks, though its cost is still high. Air interface is used in sparsely-populated areas when deployment speed is needed. Although all these media intend to bring broadband to the home, they do it differently, using transmission principles, which affect parameters such as line coding and equalization. They offer different bandwidths (less for twisted pair, highest for optical fiber) and differ in network topology (point-to-point or point-to-multi-point).

Because of complex evolving standards, proposed architectures are at least partly based on programmable platforms consisting of DSPs, standard processors, and control memories. This approach is complemented by downloadable software. Design is dominated by analog aspects. Achieving transmission performance with reasonable power consumption needs to be tackled by new structures for analog drivers, power amplifiers, ADCs, and DACs.

Three families of access technology are discussed: DSL, best-known of the broadband technologies, outpacing the others in deployment speed; wireless in the local loop (WLL) and local multipoint distribution system (LMDS); and point-to-multipoint optical (PON) offering large bandwidth.

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P. Gelsinger

1.3: Microprocessors for the New Millennium – Challenges, Opportunities and New Frontiers

Patrick P. Gelsinger

Intel Corporation, Hillsboro. OR

As designs become more complex, technology scaling more difficult, and power issues more pressing, “business as usual” no longer suffices, if the industry is to continue its long-standing tradition of microprocessor innovation. To provide means for system performance advancements and power management, there must be focus on all aspects of the computing platform – architecture, micro-architecture, bus memory, and I/O performance – much more than in the past.

Multithreading and multi-core computer micro-architectures will increase both general-purpose and networking processor MIPS. Transaction-focused server processors will benefit from large on-die caches. Special-purpose architectures and circuit techniques will be required to deliver performance with higher efficiency. Future microprocessors will evolve as integration of DSP capabilities becomes imperative to enable such applications as media-rich communications, computer vision, and speech recognition. These advances in processing natural data will lead to a change in the computing paradigm from today’s data-based, machine-based computing to tomorrow’s knowledge-based, human-based computing. As the Internet becomes more integral to businesses and consumers, there will be new uses for and users of microprocessors.

All this can be accomplished only with wired and wireless high-bandwidth Internet connectivity, driven by high-performance compute servers to fulfill the demand of computing in the Internet economy. This is computing anytime, anywhere, anyway the user wants it.

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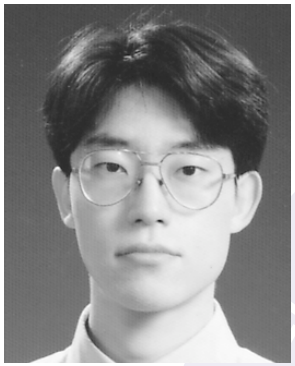

T. Cho

2.1: A 3.3V 1Gb Multi-Level NAND Flash Memory with Non-Uniform Threshold Voltage Distribution

Taehee Cho, Young-Taek Lee, Euncheol Kim, Jinwook Lee, Sunmi Choi, Seungjae Lee, Dong-Hwan Kim, Wook-Kee Han, Young-Ho Lim, Jae-Duk Lee, Jung-Dal Choi, Kang-Deog Suh

Samsung Electronics, Kyunggi, Korea

A 1Gb NAND flash memory with 2b per cell uses 0.15µm CMOS and achieves simultaneous operation of 4 independent banks with 1.6MB/s program throughput. Fusing enables changing to 512Mb 1b per cell NAND flash memory. Wordline ramping minimizes noise and peak current. Disturb mechanisms and noise related V_{TH} distribution shifts are minimized to improve read margins.

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T. Ishii

2.2: A 126.6mm² AND-Type 512Mb Flash Memory with 1.8V Power Supply

Tatsuya Ishii, Kazuyoshi Oshima, Hiroshi Sato, Satoshi Noda, Jiro Kishimoto, Hiroaki Kotani, Atsushi Nozoe, Kazunori Furusawa[1], Takayuki Yoshitake[1], Masataka Kato[1], Masahito Takahashi[1], Akihiko Sato[1], Shoji Kubono[2], Kiichi Manita[2], Kenji Koda[3], Takeshi Nakayama[3], Akira Hosogane[3]

Device Devolopment Center
[1]Semiconductor & Integrated Circuits, Hitachi Ltd., Tokyo, Japan,
[2]Hitachi ULSI Systems Corp., Tokyo, Japan, [3]Mitsubishi Electric Corp., Hyogo, Japan

A 512Mb AND-type flash memory in 0.18µm CMOS achieves 126.6mm² die size, uses a multilevel technique, and adapts to 1.8V operation. In addition, a read-modify-write mode enables programming free from pre-programmed states.

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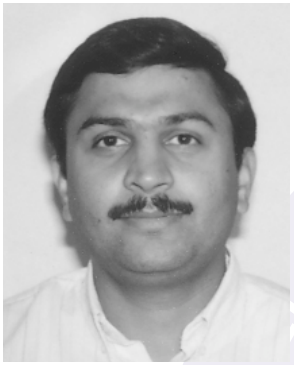

B. Pathak

2.3: A 1.8V 64Mb 100MHz Flexible Read-While-Write Flash Memory

B. Pathak, A. Cabrera, G. Christensen, A. Darwish, M. Goldman, R. Haque, J. Jorgensen, R. Kajley, T. Ly, F. Marvin, S. Monasa, Q. Nguyen, D. Pierce, A. Sendrowski, I. Sharif, H. Shimoyoshi, A. Smidt, R. Sundaram, M. Taub, W. Tran, R.Trivedi, P.Walimbe, E. Yu

Intel Corporation, Folsom, CA

A flash memory with flexible multi-partition architecture allows programming or erasing in one partition while reading from another partition. The 64Mb memory uses a 0.18µm process that has a 0.32µm^2 cell. The device has 18ns asynchronous page mode access and synchronous burst reads up to 100MHz with zero wait state.

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T. Ditewig

2.4: An Embedded 1.2V read Flash Memory Module in a 0.18µm Logic Process

Ton Ditewig[1], Roger Cuppens[1], Kuo-Lung Chen[2], Vincent Frowijn[2], Frank Jetten[2], Wim Kalkman[2], Mickael Malabry[2], Andre Slenter[2], Maurits Storms[2], Naresh Tandan[2], Stanley Teuben[2] and José Grácio[3]

[1] Philips Research Laboratories Eindhoven, The Netherlands
[2] Philips Semiconductors Eindhoven, The Netherlands
[3] Presently at TIM AG, Thalwil, Switzerland

An embedded flash memory module has 1.2V read capability and a 1.5V program/erase capability. The flash cell is 2-transistor FN-NOR in a 0.18µm logic process. Design techniques improve observability and reduce test time.

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C. Ohno

2.5: A Highly-Reliable 1T1C 1Mb FRAM with Novel Ferro-Programmable Redundancy Scheme

Chikai Ohno, Hirokazu Yamazaki, Hideaki Suzuki, Eiichi Nagai, Hisashi Miyazawa*, Kaoru Saigoh*, Tatsuya Yamazaki*, Yeonbae Chung, William Kraus**, Don Verhaeghe**, George Argos**, John Walbert**, Sanjay Mitra****

Fujitsu Limited, Tokyo

*Iwate, Japan, **Ramtron International Corp., Colorado Springs, CO

Two key design techniques improve margins of the 1T1C, 1Mb FeRAM. One is a redundancy scheme utilizing the same ferroelectric capacitor as used in the memory cell, which can be implemented without additional process steps. The other is an externally controllable dummy cell reference that mimics memory cell properties and also finds weak cells prior to repair.

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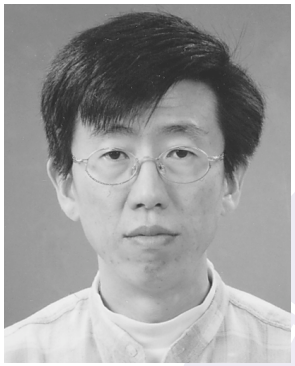

B. Jeon

2.6: A Nonvolatile Ferroelectric RAM with Common-Plate Folded Bit-line Cell and Enhanced Data Sensing Scheme

Byung-Gil Jeon, Mun-Kyu Choi, Yoonjong Song, Kinam Kim

Samsung Electronics, Kiheung, Korea

A 4Mb 1T1C FeRAM with a common-plate folded bit-line architecture achieves low noise without cell area penalty in nonvolatile ferroelectric RAM. The decoder of common plate scheme reduces area to about 62% that of a conventional separate-plate scheme. The chip area is reduced by 9.2% to 111 mm^2. The bit-line capacitance imbalance is resolved without speed loss or area penalty.

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D. Takashima

2.7: A 76mm² 8Mb Chain Ferroelectric Memory

Daisaburo Takashima, Yoshiaki Takeuchi, Tadashi Miyakawa, Yasuo Itoh, Ryu Ogiwara, Masahiro Kamoshida, Katsuhiko Hoya, Sumiko Mano Doumae, Tohru Ozaki, Hiroyuki Kanaya, Masami Aoki, Koji Yamakawa, Iwao Kunishima, Yukihito Oowaki

Semiconductor Company, Toshiba Corp., Yokohama, Japan

An 8Mb chain FeRAM uses 0.25µm 2-metal CMOS technology. A one-pitch-shift cell realizes 5.2µm² cell area. A chain architecture with a hierarchical wordline scheme gives 76mm² die. Random access time is 40ns, and cycle time is 70ns at 3.0V.

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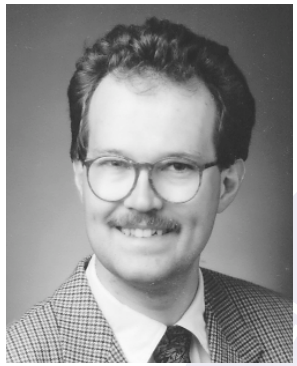

T. Burger

3.1: A 13.5mW, 185MSample/s ΣΔ Modulator for UMTS/GSM Dual-Standard IF Reception

Thomas Burger and Qiuting Huang

Integrated Systems Laboratory, Swiss Federal Institute of Technology (ETH), Zurich, Switzerland

To accommodate drastically different symbol rates, signal bandwidth and SNR requirements between WCDMA and GSM, the IF frequency, sample-rate and converter architecture are optimized for a dual-standard ΣΔ modulator. In the system and circuit design, attention is given to low power consumption to achive 135mW at 18MSample/s. Measured dynamic range is 53dB for WCDMA and 84dB for GSM.

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O. Oliaei

3.2: A 5mW ΣΔ Modulator with 84dB Dynamic Range for GSM/EDGE

Omid Oliaei, Patrick Clement*, Philippe Gorisse

Motorola SPS, Toulouse, France, *Geneva, Switzerland

A ΣΔ modulator in 0.35µm technology for GSM/EDGE applications has 13MHz clock. Frequency is 13MHz. The modulator achieves 84dB dynamic range and 82dB peak SNDR over 180kHz bandwidth. Power dissipation is 5mW from 1.8/2.4V supplies. Active area is 0.4mm^2.

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L. Breems

3.3: A Quadrature Data Dependent DEM Algorithm to Improve Image Rejection of a Complex ΣΔ Modulator

Lucien J. Breems, E. Carel Dijkmans and Johan H. Huijsing[1]

Philips Research Laboratories, Eindhoven, The Netherlands
[1]Delft University of Technology, Delft, The Netherlands

A data-dependent DEM algorithm is controlled by the quadrature bitstreams of a complex ΣΔ modulator. The quadrature feedback paths of the modulator are dynamically matched, without increasing the in-band noise. Test chips with an initial 20% mismatch have a typical image rejection ratio of 61dB with DEM.

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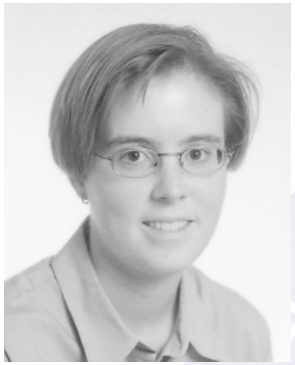

K. Vleugels

3.4: A 2.5V Broadband Multi-Bit ΣΔ Modulator with 95dB Dynamic Range

Katelijn Vleugels, Shahriar Rabii, Bruce A. Wooley

Center for Integrated Systems, Stanford University, CA

A cascaded multi-bit ΣΔ modulator uses double sampling to achieve a conversion rate of at least 4MSample/s at an oversampling ratio of 16. Partitioned data-weighted averaging extends the dynamic range to 95dB. The circuit, integrated in 0.5µm CMOS, dissipates 150mW from a 2.5V supply.

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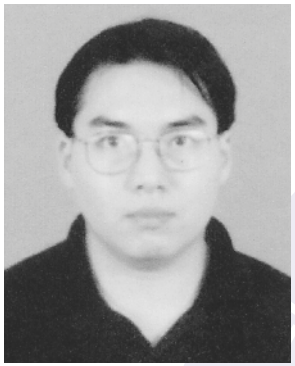

V. Cheung

3.5: A 1V 10.7MHz Switched-Opamp Bandpass ΣΔ Modulator Using Double-Sampling Finite-Gain-Compensation Technique

Vincent S. L. Cheung, Howard C. Luong and W. H. Ki

Dept. of EEE, The Hong Kong University of Science and Technology

A 1V 10.7MHz switched-opamp bandpass ΣΔ modulator uses modified double-sampling finite-gain-compensation. In a standard 0.35µm CMOS process at 1V supply, the modulator achieves 42.8MHz effective sampling frequency with 42.3dB peak SNDR while dissipating 12mW in 1.3mm^2 chip area.

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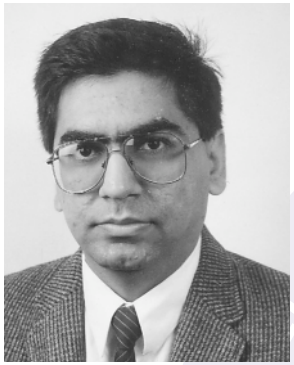

K. Gulati

3.6: A Low-Power Reconfigurable Analog-to-Digital Converter

Kush Gulati and Hae-Seung Lee

Massachusetts Institute of Technology, Cambridge MA

A reconfigurable analog-to-digital converter digitizes signals over a 1Hz -10MHz bandwidth and 6 to 16b resolution with adaptive power consumption. The converter achieves this by reconfiguring between pipeline and ΔΣ architectures and adjusting circuit parameters and bias currents.

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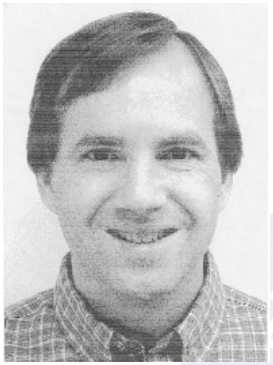

W. Ellersick

4.1: A Serial-Link Transceiver Based on 8GSample/s A/D and D/A Converters in 0.25µm CMOS

William Ellersick[1,3], Chih-Kong Ken Yang[2], Vladimir Stojanovic[1], Siamak Modjtahedi[2], Mark A. Horowitz[1]

[1]Stanford University, Stanford, CA, [2]University of California, Los Angeles, CA , [3]Analog Devices, Inc., Wilmington, MA

On-chip VCOs generate 16 clock phases that drive an 8-way interleaved 4b A/D input receiver and an 8-way interleaved 8b D/A transmitter. 4GHz bandwidth is achieved by inductors that distribute the I/O capacitance and a transmit equalizer. Digital calibration adjusts the sample timing to 10ps, the input and output accuracy to <1 LSB and 3 LSBs, respectively.

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T. Tanahashi

4.2: A 2Gb/s 21CH Low-Latency Transceiver Circuit for Inter-Processor Communication

Toshio Tanahashi, Masakazu Kurisu, Hiroshi Yamaguchi, Takaaki Nedachi, Masahiro Arai, Shiro Tomari, Tsutomu Matsuzaki, Kazuyuki Nakamura, Muneo Fukaishi, Shinzo Naramoto[1], Takanori Sato[1]

NEC Corp., Tokyo, Japan, [1]NEC Engineering Ltd.

A 20-data-channel transceiver with a control channel allows uncoded data transfer with 13ns latency. A digital DLL with a ring-interpolator tracks phase with 20ps resolution. A pre-emphasis driver enables 2Gb/s transmission per channel over a 7m cable at 1.5V. The effective full-duplex bandwidth reaches 10GB/s.

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M. Haycock

4.3: 3.2GHz 6.4Gb/s/wire Signaling in 0.18µm CMOS

Matthew Haycock, Randy Mooney

Intel Corp., Hillsboro, OR

Simultaneous bidirectional signaling provides 6.4Gb/s/wire with random data on a 22b point-to-point bus over 15cm on a PCB. The signaling rate decreases to 2.4Gb/s/wire over 122cm through 2 connectors. The I/O circuits have closed-loop slew rate control and are part of a 6.6M transistor router component that consumes 21W, packaged in a 31x31mm^2 OLGA substrate.

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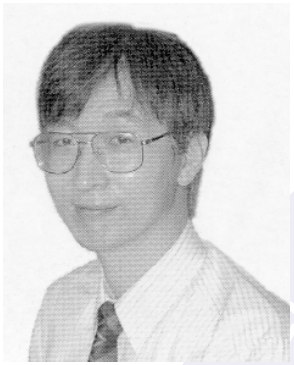

H. Tamura

4.4: 5Gb/s Bidirectional Balanced-Line Link Compliant with Plesiochronous Clocking

Hirotaka Tamura, Masaya Kibune, Yuji Takahashi, Yoshiyasu Doi, Takuya Chiba[1], Hirohito Higashi, Hideki Takauchi, Hideki Ishida, Kohtaroh Gotoh

Fujitsu Laboratories LTD., Kawasaki, Japan, [1]Fujitsu Hokkaido Digital Technology, Hokkaido, Japan

A 6ns-latency 12mW 5Gb/s bidirectional link for short-haul (<5m) balanced lines uses an on-chip switched-capacitor hybrid with echo-canceling capability. The clock-recovery circuit, based on a phase interpolator, makes the link tolerant to a 100ppm difference between the frequencies of the transmit and receive clocks.

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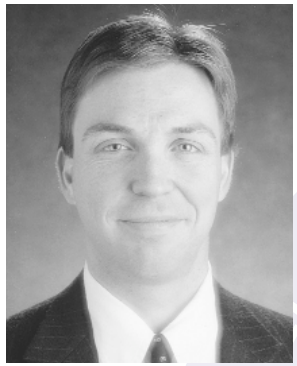

J. Zerbe

4.5: A 2Gb/s/pin 4-PAM Parallel Bus Interface with Transmit Crosstalk Cancellation Equalization and Integrating Receivers

Jared L. Zerbe, Pak S. Chau, Carl W Werner, William F. Stonecypher, H. J. Liaw, Gong Jong Yeh, Timothy P. Thrush, Scott C. Best, Kevin S. Donnelly

Rambus, Mountain View, CA

A 2Gb/s/pin single-ended 4-PAM parallel bus interface uses transmit crosstalk cancellation and equalization techniques as well as integrating data receivers to improve system margin in low-cost packaging despite inherent coupling noise and data distortion.

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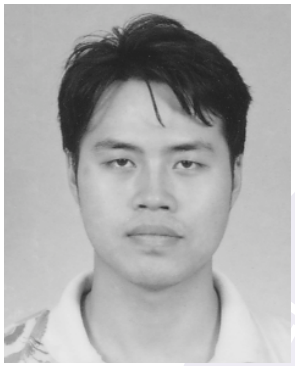

K. Kim

4.6: Digitally-Controlled DLL and I/O Circuits for 500Mb/s/pin x16 DDR SDRAM

Jung-Bae Lee, Kyu-hyoun Kim, Changsik Yoo, Sangbo Lee, One-Gyun Na, Chan-Yong Lee, Ho-Young Song, Jong-Soo Lee, Zi-hyoun Lee, Ki-woong Yeom, Hoi-Joo Chung, Il-Won Seo, Moo-Sung Chae, Yun-Ho Choi, Soo-In Cho

DRAM Development Group, Samsung Electronics,
Yongin-City, Kyunggi-Do, Korea

DLL and improved I/O circuits are for 500Mb/s/pin DDR SDRAM. This digitally-controlled DLL has inherent duty cycle correction capability, enabling fast re-locking upon standby-mode exit. Data input circuits, such as internal delay control and digital sense amplifier, reduce setup/hold window to 0.3ns. The output data driver has 62% decreased pattern-dependent skew.

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S. Sidiropoulos

4.7: Circuit Design for a 2.2GB/s Memory Interface

Stefanos Sidiropoulos, Abhijit Abhyankar, Catherin Chen, Ken Chang, Tsu-Ju Chin, Neal Hays, Jun Kim, Ying Li, Grace Tsang, Anthony Wong, Don Stark

Rambus Inc., Mountain View, CA

A 2.2GB/s signaling interface for main memory uses a DLL that allows for in-system timing calibration with 1.4° resolution, and output drivers with limited positive feedback to increase voltage margin. In a 0.25µm CMOS process, the prototype chips operate to 2.6GB/s.

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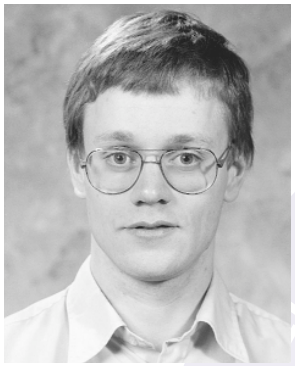

P. Larsson

5.1: An Offset-Cancelled CMOS Clock Recovery/Demux with a Half-Rate Linear Phase Detector for 2.5Gb/s Optical Communication

Patrik Larsson

Bell Labs, Lucent Technologies, Holmdel, NJ

A 2.5Gb/s optical receiver clock-recovery circuit in 0.25µm CMOS features 4mV sensitivity and offset cancellation to enable an integrated limiting amplifier. A linear phase detector using a half-rate clock relaxes speed requirements. An active on-chip loop filter capacitor gives <0.1dB jitter peaking.

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A. Momtaz

5.2: Fully-Integrated SONET OC48 Transceiver in Standard CMOS

Afshin Momtaz, Jun Cao, Mario Caresosa, Armond Hairapitian, David Chung, Kambiz Vakilian, Mike Green, Ben Tan, Keh-Chee Jen, Ichiro Fujimori, German Gutierrez, Yijun Cai

Broadcom Corp, Irvine, CA

A fully-integrated transceiver in standard 0.18µm CMOS exceeds all SONET OC-48 requirements. The serial interfaces are 2.488 or 2.667Gb/s CML and the parallel ones are 622 or 666Mb/s LVDS. The output clock rms jitter is 1ps and total power consumption including all the input/output interfaces is 500mW.

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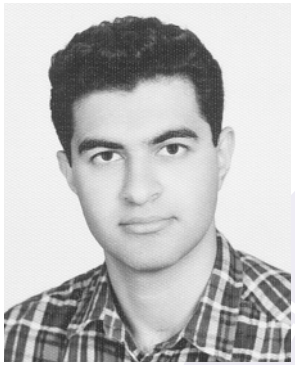

J. Savoj

5.3: A 10Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection

Jafar Savoj, Behzad Razavi

Electrical Engineering Department, University of California, Los Angeles, CA

A 10Gb/s phase-locked clock and data recovery circuit incorporates a multiphase LC oscillator and a half-rate phase/frequency detector with automatic data retiming. In 0.18µm CMOS technology, the circuit exhibits 1.43GHz capture range and 0.8ps rms jitter with length 2^{23}-1 PRBS. The power dissipation is 91mW from a 1.8V supply.

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M. Loinaz

5.4: A 10Gb/s 16:1 Multiplexer and 10GHz Clock Synthesizer in 0.25µm SiGe BiCMOS

Hong-Ih Cong[1], Shawn M. Logan[2], Marc J. Loinaz[3], Kenneth J. O'Brien[4], Elizabeth E. Perry[5], Gary D. Polhemus[4], John E. Scoggins[4], Kenneth P. Snowdon[4], Michael G. Ward[4]

Agere Systems, [1]Murray Hill, NJ, [2]North Andover, MA, [3]Holmdel, NJ, [4]South Portland, ME, [5]Reading, PA

A 10Gb/s 16:1 multiplexer, 10GHz clock generator, and 6×16b input data buffer are integrated in SiGe BiCMOS. The chip exhibits SONET generated jitter of $0.048UI_{pp}$ with 0.04dB maximum jitter peaking and dissipates 1.6W from 3.3V. The input data buffer accommodates ±2.4ns input data phase drift at 622Mb/s.

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S. Ueno

5.5: A Single-Chip 10Gb/s Transceiver LSI using SiGe SOI/BiCMOS

Satoshi Ueno, Keiki Watanabe, Takahiro Kato, Takashi Shinohara[1], Kouji Mikami[1], Takashi Hashimoto, Atsushi Takai[2], Katsuyoshi Washio[3], Ryoji Takeyari[3], Takashi Harada

Device Development Center, Hitachi, Ltd., Ome, Tokyo, Japan
[1]Hitachi ULSI Systems Co., Ltd., Ome, Tokyo, Japan, [2]Telecommunication Systems Div., Hitachi, Ltd., Yokohama, Kanagawa, Japan, [3]Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo, Japan

A fully-integrated single-chip SiGe SOI/BiCMOS transceiver LSI for 10Gb/s applications combines 4b FIFO, 10GHz PLL, 16:1 MUX, 10Gb/s input data decision circuit, clock and data-recovery circuit, 1:16 DeMUX, data loop back function, and self-testing using 2^{23}-1 PRBS generator. The die is 5.6x5.3mm^2 and consumes 2.6W from 3.3/2.5V.

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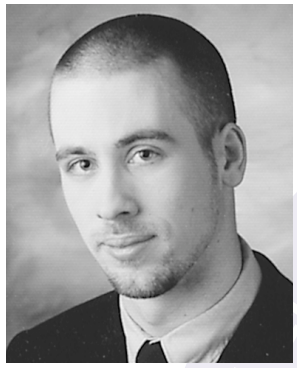

M. Reinhold

5.6: 40Gb/s Clock and Data Recovery / 1:4 DEMUX IC in SiGe Technology

Mario Reinhold, Claus Dorschky, Rajasekhar Pullela[1], Eduard Rose, Peter Mayer, Peter Paschke, Yves Baeyens[2], John-Paul Mattia[3], Frank Kunz

Lucent Technologies, Optical Networking Group, Nuremberg, Germany
[2]Lucent Technologies, Bell Labs, Murray Hill, NJ, [1]now with Gtran Inc., Westlake Village, CA, [3]now with BigBear Networks, Sunnyvale, CA

A 40Gb/s clock and data recovery (CDR) IC with 1:4 demultiplexer (DEMUX) is fabricated in a SiGe technology. The architecture provides robust operation combined with a high level of integration, dissipating 4.8W from a 5.5 V supply.

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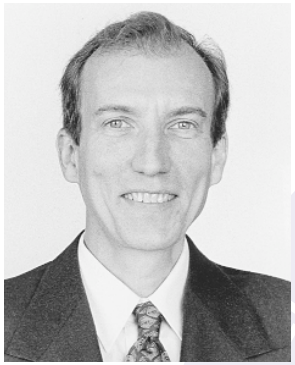

S. Kleinfelder

6.1: A 10kframes/s 0.18µm CMOS Digital Pixel Sensor with Pixel-Level Memory

Stuart Kleinfelder, SukHwan Lim, Xinqiao Liu, Abbas El Gamal

Stanford University, Stanford CA

A 352x288 pixel CMOS image sensor with pixel-level single-slope ADC and 8b 3T DRAM cells achieves 9.4x9.4µm^2 pixel in standard 0.18µm CMOS. Continuous 10kframes/s (1Gpixels/s) 8b per pixel snapshot image acquisition is achieved with 0.1% rms temporal noise and 0.18% rms FPN.

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J. Hurwitz

6.2: A Miniature Imaging Module for Mobile Applications

Jed Hurwitz, Stewart G Smith, Andrew A Murray, Peter B Denyer, Jim Thomson, Stuart Anderson, Ed Duncan, Andrew Kinsey, Brian Paisley, Pierre-Francois Pugibet, Eric Christison, Brian Laffoley, Mark Panaghiston, Stephen Bradshaw, Julien Vittu, Remi Brechignac and Keith M Findlater.

STMicroelectronics, Edinburgh, UK

A miniature mobile imaging module combines a 0.5µm CMOS CIF imager with a 0.18µm co-processor within a compact lensed package. It provides 15frames/s ITU-Rec.656 data with 50mW consumption. Automatic flicker-detection is one of the features that help the camera function in a mobile application.

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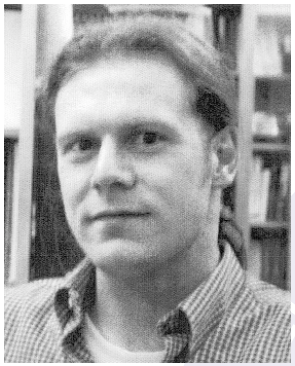

E. Culurciello

6.3: Arbitrated Address Event Representation Digital Image Sensor

Eugenio Culurciello[1], Ralph Etienne-Cummings[1], Kwabena Boahen[2]

[1]Dept. of ECE, Johns Hopkins University, Baltimore, MD 21218,
[2]Bioengineering Department, University of Pennsylvania, Philadelphia, PA 19104

80x60 (1/8 VGA) address event imager in 0.6µm CMOS converts light intensity into a one-bit code (a spike). The read-out of each spike is initiated by the pixel. The dynamic range is 200dB for a pixel and 120dB for the array. It uses 3.4mW at a spike rate of 200kHz. It is capable of 8.3k effective frames/s.

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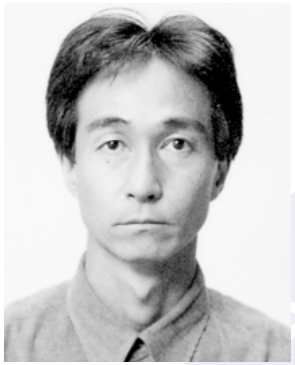

S. Yoshimura

6.4: A 48kframes/s CMOS Image Sensor for Real-Time 3-D Sensing and Motion Detection

Shinichi Yoshimura, Toshinobu Sugiyama[1], Kazuya Yonemoto[2], Kazuhiko Ueda[3]

Sony-Kihara Research Center, Inc., Tokyo, Japan
[1]Microsystem Div., Imaging Device Group, SNC, Sony Corp., Kanagawa, Japan, [2]DI Div., Personal Video Co., PNC, Sony Corp., Tokyo, Japan
[3]SDS Lab., INT Labs., Sony Corp., Tokyo, Japan

A CMOS image sensor with 192x124 pixels realizes video-rate range sensing with 500µm depth resolution, motion detection, and 12b digital image output. Each pixel consists of four current copier cells as a frame memory block and a chopper comparator. The imager operates at 48kframes/s maximum rate and dissipates 1.6W for range sensing and 2W for digital imaging at 3.3V in a 0.35mm process.

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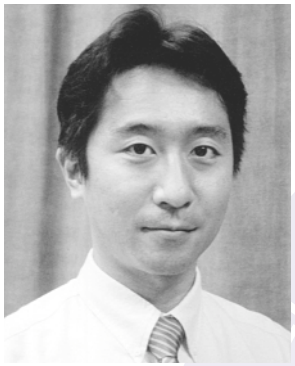

H. Yamashita

6.5: A 128x128 CMOS Imager with 4x128 Bit-Serial Column-Parallel PE Array

Hirofumi Yamashita, Charles G. Sodini*

Toshiba Corporation, Yokohama, Japan
*Massachusetts Institute of Technology, Cambridge, MA

A 4x128 fine-grained bit-serial processing element array configured with four 1x128 SIMD processors is embedded in 128x128 pixel CMOS imager columns. The prototype imager chip performs ~220operations/pixel at 20MHz clock, which potentially affords pixel-rate color processing for VGA format image.

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Y. Muramatsu

6.6: A Signal-Processing CMOS Image Sensor using a Simple Analog Operation

Yoshinori Muramatsu, Susumu Kurosawa, Masayuki Furumiya, Hiroaki Ohkubo, Yasutaka Nakashiba

NEC Corp., Kanagawa, Japan

A high-density CMOS image sensor has a normal mode and three signal-processing function modes: wide dynamic-range mode, motion-detection mode, and edge-extraction mode. Small pixel and real-time operation are achieved by using a 4-transistor pixel scheme and column-parallel on-chip analog operation.

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O. Yadid-Pecht

6.7: Autoscaling CMOS APS with Customized Increase of Dynamic Range

Orly Yadid-Pecht and Alexander Belenky

Electrical and Computer Engineering Department, Ben-Gurion University, Beer-Sheva, Israel

A 64x64 CMOS active pixel sensor uses autoscaling and a floating-point representation to achieve wide dynamic-range linear output. The chip features a new architecture enabling a customized number of additional bits per pixel readout, with minimal effect on the sensor spatial and temporal resolution.

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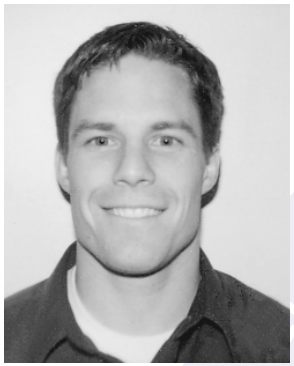

T. Gardner

7.1: Genetic Applets: Biological Integrated Circuits for Cellular Control

Timothy S. Gardner

Cellicon Biotechnologies, Inc., Boston, MA

Technological advances in the biological sciences, coupled with increasing technical and economic challenges for silicon-based computing, generate interest in biocomputing. A genetic flip-flop and a genetic clock, recently implemented bacterial cells, may form the basic elements of a biochemical integrated circuit that operates in a living cell.

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M. Reed

7.2: The Design and Measurement of Molecular Electronic Switches and Memories

M. A. Reed[1], J. Chen[1], D. W. Price[2], A. M. Rawlett[2], J. M. Tour[2], W. Wang[1]

[1]Departments of Electrical Engineering, Applied Physics, and Physics, Yale University, New Haven, CT, [2]Department of Chemistry and Center for Nanoscale Science and Technology, Rice University, Houston, TX

Molecular-scale devices have recently become possible with self-assembly techniques. Examples of a number of simple molecular devices and circuits include a negative-resistance device that exhibits peak-to-valley ratios exceeding 1000:1 and a molecular memory cell with refresh times exceeding 10 minutes.

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K. Rim

7.3: Strained Si Surface Channel MOSFETS for High-Performance CMOS Technology

Kern (Ken) Rim

IBM T. J. Watson Research Center, Yorktown Heights, NY

Biaxial tension enhances in-plane transport of both electrons and holes in silicon, and can improve the current drive of CMOS devices independent of geometric scaling and electrostatic design. Device performance enhancements and issues to be addressed before the realization of strained Si CMOS technology are discussed.

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S. Tang

7.4: FinFET - A Quasi-Planar Double-Gate MOSFET

Stephen H. Tang, Leland Chang, Nick Lindert, Yang-Kyu Choi, Wen-Chin Lee[1], Xuejue Huang, Vivek Subramanian, Jeffrey Bokor, Tsu-Jae King, Chenming Hu

Dept. of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, [1]Now with Intel Corp., Hillsboro, OR.

The quasi-planar FinFET structure has device characteristics similar to those of the conventional MOSFET. Inserting FinFET into CMOS technology requires no change in circuit architecture or layout/design tools, providing a smooth transition to post-planar CMOS technology. 2D mixed-mode simulations show FinFET circuit performance exceeds that of advanced single-gate MOSFETs.

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R. Ruby

7.5: Ultra-Miniature, High-Q Filters and Duplexers Using FBAR Technology

Richard Ruby, Paul Bradley, John Larson III, Yury Oshmyansky, Domingo Figueredo

Agilent Technologies, Inc., Newark, CA

An ultra-miniature PCS duplexer uses thin-film bulk acoustic resonator technology. FBAR resonators are made using aluminum nitride for piezoelectric material and silicon as substrate. It has better than -52dB rejection of the Rx filter in the Tx band and pass-band insertion losses are on the order of 2dB (Tx) and 3dB (Rx). Performance is comparable to that of much larger ceramic duplexers.

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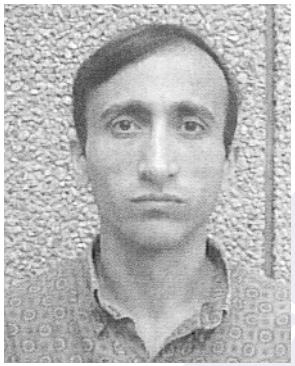

P. Naji

7.6: A 256kb 3.0V 1T1MTJ Nonvolatile Magnetoresistive RAM

Peter K. Naji, Mark Durlam, Saied Tehrani, John Calder, Mark F. DeHerrera

Motorola Labs, Physical Sciences Research Labs, Chandler, AZ

A 256kb nonvolatile magnetoresistive RAM (MRAM) is based on a memory cell defined by a single transistor (1T) and a single magnetic tunnel junction (MTJ) with read and write cycles <50ns. The memory organization is 16kx16. Measured read power consumption is 24mW at 3V and 20MHz.

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M. Choi

8.1: A 6b 1.3GSample/s A/D Converter in 0.35µm CMOS

Michael Choi, Asad A. Abidi

Electrical Engineering Department, University of California, Los Angeles, CA

Using array averaging and a wideband track-and-hold, a 6b flash ADC achieves better than 5.5 effective bits for input frequencies to 600MHz at 1GSample/s, and 5 effective bits for 650MHz input at 1.3GSample/s. It consumes 500mW from 3.3V and occupies 0.8mm^2 in 0.35µm CMOS.

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G. Geelen

8.2: A 6b 1.1GSample/s CMOS A/D Converter

Govert Geelen

Philips Semiconductors, Eindhoven, The Netherlands

A 6b flash ADC incorporating an averaging/interpolating technique achieves 1.1GSample/s in 0.35µm 3.3V CMOS. Measured ENOB is >5b up to 450MHz input at 900MSample/s. Chip area is 0.35mm^2 and power consumption is 300mW.

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Y. Park

8.3: A 1.8V 10b 100MSample/s CMOS Pipelined ADC with 1.8V Power Supply

Yong-In Park, S. Karthikeyan, Frank Tsay, Eduardo Bartolome

Texas Instruments Inc., Dallas, TX

A 100MHz ADC for low-power applications uses a 0.18µm digital CMOS process. The design achieves 9.4 ENOB for a 50MHz input at full sampling rate, and consumes a total of 180mW with 2.5mm^2 core in a single 1.8V power supply.

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H. van der Ploeg

8.4: A 2.5V 12b 54MSample/s 0.25µm CMOS ADC in 1mm²

Hendrik van der Ploeg, Gian Hoogzaad, Henk A.H. Termeer, Maarten Vertregt, Raf L.J. Roovers

Philips Research Laboratories, Eindhoven, The Netherlands

Background digital offset extraction and analog compensation remove offset of the critical analog components. The calibrated two-step ADC achieves -70dB THD in the Nyquist band with a 2.5V supply. The ADC in 0.25µm CMOS measures 1.0mm² and dissipates 295mW.

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D. Kelly

8.5: A 3V 14b 75MSample/s CMOS ADC with 85dB SFDR at Nyquist

Dan Kelly, Will Yang, Iuri Mehr, Mark Sayuk, Larry Singer

Analog Devices Inc., Wilmington, MA

A 14b multi-bit pipeline ADC achieves 0.6LSB DNL and 2LSB INL without calibration. Typical SNR is 73dB, while SFDR is >85dB for input frequency up to Nyquist. The 7.8mm^2 ADC in 0.35µm double-poly triple-metal process operates with a 2.7V to 3.6V power supply, and consumes 340mW at 3V.

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P. Yu

8.6: A 14b 40MSample/s Pipelined ADC with DFCA

Paul C. Yu, Shereef Shehata, Ashutosh Joharapurkar, Pankaj Chugh, Alexander R. Bugeja, Xiaohong Du, Sung-Ung Kwak, Yiannis Papantonopoulous, Turker Kuyel

Texas Instruments, Inc., Dallas, TX

A DAC and feedback capacitor averaging (DFCA) used in a pipelined ADC achieves 84dB SFDR and 74db SNR. External mismatch noise cancellation digitally improves SNR. Excluding output drivers, the 0.6µm double-poly BiCMOS ADC dissipates 860mW from 3.3V supply.

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T. Hashimoto

9.1: A 90mW MPEG4 Video Codec LSI with the Capability for Core Profile

Takashi Hashimoto, Shun-ichi Kuromaru, Masatoshi Matsuo, Yasuo Kohashi, Toshihiro Moriiwa, Ken-ichi Ishida, Satoshi Kajita, Masahiro Ohashi, Masayoshi Toujima, Tsuyoshi Nakamura, Mana Hamada, Tomonori Yonezawa, Takahiro Kondo, Kohkichi Hashimoto, Yuji Sugisawa, Hiroki Otsuki, Miki Arita, Hiromasa Nakajima, Hitoshi Fujimoto, Junji Michiyama, Yasuo Iizuka, Hiroyuki Komori, Shintaro Nakatani[1], Hiroaki Toida[1], Toshiya Takahashi[1], Hiroyuki Ito[2], Takeshi Yukitake[2]

Matsushita Electric Industrial Co., Ltd., Fukuoka, Japan, [1]Osaka, Japan, [2]Matsushita Communication Industrial Co., Ltd., Kanagawa, Japan

A single-chip MPEG4 video codec LSI with 20Mb embedded DRAM performs a QCIF 15Hz H.263 codec, a Simple at L1 codec, and Core at L1 decoding. It consumes 90mW at 54MHz. This chip integrates a programmable DSP, 8 dedicated hardware engines, and interface units on a 75.68mm^2 die using 0.18µm 1.8V quad-metal CMOS technology.

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C-W. Yoon

9.2: A 80/20MHz 160mW Multimedia Processor integrated with Embedded DRAM, MPEG-4 Accelerator, and 3D Rendering Engine for Mobile Applications

Chi-Weon Yoon, Ramchan Woo, Jeonghoon Kook, Se-Joong Lee, Kangmin Lee, Young-Don Bae, In-Cheol Park and Hoi-Jun Yoo

Dept. of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea

A 84mm^2 160mW programmable processor in 0.18µm EML technology consists of 32b RISC with MAC, 20MHz motion compensation accelerator for MPEG-4 at SP, 3D rendering engine with 2.2Mpolygon/s at 20MHz, and 7.125Mb embedded DRAM with single bit-line writing scheme.

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T. Watanabe

9.3: One Chip 15frame/s Mega-Pixel Real-time Image Processor

Hideki Yamauchi, Shigeyuki Okada, Yuh Matsuda, Tsugio Mori, Tsuyoshi Watanabe, Shin'ichiro Okada, Akio Kobayashi, Isao Ogura, Yasoo Harada

Sanyo Electric Co., Ltd., Gifu, Japan

A one-chip 15frame/s mega-pixel real time image processor. for mobile multimedia applications is presented. It contains mega-pixel CCD signal processing, a motion-JPEG/MPEG2 image compression/decompression engine, a RISC-CPU, an NTSC encoder, a SDRAM controller and peripheral interfaces.

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T. Koyama

9.4: A 250MHz Single-Chip Multiprocessor for A/V Signal Processing

Tatsuya Koyama, Eiji Iwata, Hiroshi Yoshikawa, Hirokazu Hanaki, Kouichi Hasegawa, Makoto Aoki, Masahiro Yasue, Thomas Schrobenhauser[1], Masatoshi Aikawa, Ichiro Kumata, Hideki Koyanagi

Semiconductor Network Company, Sony Corp., Tokyo, Japan, [1]System-LSI Laboratory, Sony US Research Labs, California, USA

A 250MHz single-chip multiprocessor integrates four CPUs with multimedia extended instructions in 0.25µm CMOS and consumes 2.4W at 2.5V. This chip exploits both coarse- and fine-grained parallelism in A/V signal processing and implements various codec standards such as multi-channel MPEG2 (MP at ML) video decoding.

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Y. Kondo

9.5: A 4GOPS 3Way-VLIW Image Recognition Processor based on a Configurable Media-Processor

Yoshihiasa Kondo, Takashi Miyamori, Tomoko Kitazawa, Satoshi Inoue, Hiroyuki Takano, Isao Katayama, Kunihiko Yahagi, Akihiro Ooue, Takanori Tamai, Kazuyoshi Kohno, Youji Asao, Hiroyuki Fujimura, Hironori Uetani, Youichi Inoue, Shigehiro Asano, Yukimasa Miyamoto, Akira Yamaga, Yoshio Masubuchi, Tohru Furuyama

Toshiba Corp., Kanagawa, Japan

A 4GOPS 3-way VLIW image-recognition processor for an automobile system is based on a configurable media-processor which enables design-time configuration to optimize for a specific application. It uses a 0.25µm CMOS process with a standard-cell design method.

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A. Khan

9.6: A 150MHz Graphics Rendering Processor with 256Mb Embedded DRAM

Aurangzeb K. Khan+, Hidetaka Magoshi*, Tadashi Matsumoto#, Jun-ichi Fujita, Makoto Furuhashi*, Masatoshi Imai**, Yoshikazu Kurose#, Morio Sato#, Katsuhiko Sato#, Yujiro Yamashita#, Kinying Kwan+, Duc-Ngoc Le+, John H. Yu+, Trung Nguyen+, Steven Yang+, Allen Tsou+, King Chow+, John Shen+, Min Li+, Jun Li+, Hong Zhao+, Kenji Yoshida+**

+ Altius Solutions, Inc., Santa Clara, CA , * Sony Computer Entertainment Inc., Tokyo, Japan, # Sony Corp., Semiconductor Network Co., Tokyo, Japan, ** Sony Kihara Research Center Inc. , Tokyo, Japan

A 150MHz graphics rendering processor with an integrated 256Mb embedded DRAM, delivers a rendering rate of 75M polygons/s. 287.5 M transistors are integrated on a 21.3 x 21.7mm^2 die in a 0.18µm 6-level-metal CMOS process. Several design methodologies are used.

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T. Kuo

10.1: A 1.5W Class-F RF Power Amplifier in 0.2µm CMOS Technology

Timothy C. Kuo, Bruce B. Lusignan*

Philips Semiconductors, San Jose, CA, *Stanford University, Stanford, CA

Design considerations for deep-sub-micron RF CMOS power amplifier emphasize high knee voltage design and CMOS breakdown. A square-wave driver takes advantage of CMOS. In 0.2µm CMOS, the 1x2mm^2 PA delivers 1.5W output at 900MHz with 43% PAE from a 3V supply.

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A. Shirvani

10.2: A CMOS RF Power Amplifier with Parallel Amplification for Efficient Power Control

Alireza Shirvani, David K. Su, Bruce A. Wooley

Center for Integrated Systems, Stanford University, Stanford, CA

A 0.25µm CMOS RF power amplifier uses parallel amplification to provide an output power adjustment range of 7mW to 300mW. The 2.37mm^2 amplifier achieves 49% maximum power-added-efficiency (PAE) and maintains a PAE >43% over 70% of the power range.

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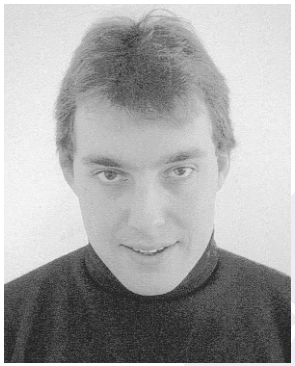

C. Fallesen

10.3: A 1W 0.35µm CMOS Power Amplifier for GSM-1800 with 45% PAE

Carsten Fallesen, Per Asbeck

Nokia Denmark A/S, Copenhagen, Denmark

A highly-integrated power amplifier in 0.35µm CMOS occupies 1.9mm^2 and features class AB operation with 31.2dBm output power at 1730MHz, and 45% maximum power added efficiency.

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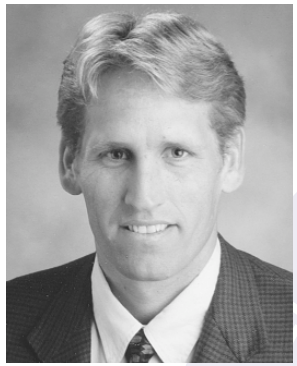

J. Weldon

10.4: A 1.75GHz Highly-Integrated Narrow-Band CMOS Transmitter with Harmonic-Rejection Mixers

Jeffrey A. Weldon, Jacques C. Rudell, Li Lin[1], R. Sekhar Narayanaswami, Masanori Otsuka[2], Sebastien Dedieu[3], Luns Tee, King-Chun Tsai, Cheol-Woong Lee, Paul R. Gray

University of California, Berkeley CA, [1]Broadcom, San Jose, CA, [2]Hitachi, Tokyo, Japan, [3]STMicroelectronics, Grenoble, France

A 1.75GHz transmitter with harmonic and double image reject mixer integrates the full signal path from the DAC to the RF output with two frequency synthesizers in a 0.35µm double-poly five-metal CMOS process. The IC consumes 151mA from a 3V supply and achieves 1.3° rms phase error. Active area is 3x9.9mm^2.

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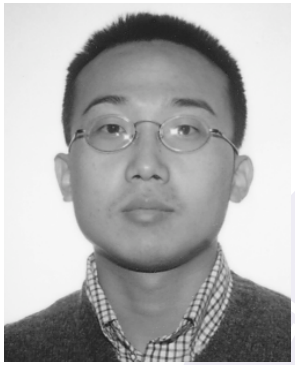

Y. Ding

10.5: A +18dBm IIP3 LNA in 0.35µm CMOS

Yongwang Ding, Ramesh Harjani

Department of ECE, University of Minnesota, Minneapolis, MN

A feedforward linearization technique for RF CMOS LNAs makes feasible up to 40dB output linearity improvement in current CMOS processes. A high-linearity LNA with +18dBm IIP3 in a 0.35µm CMOS process shows little impact on power, noise, and gain.

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F. Martin

10.6: A Wideband 1.3GHz PLL for Transmit Remodulation Suppression

Frederick L. Martin, Ron C. Alford, Jeremy Marks, Gregory S. Raven, Jeffrey Rollman

Motorola, Inc., Plantation, FL

A 1.3GHz 0.5µm BiCMOS offset PLL realizes -132dBc/Hz in-band phase noise while reducing re-radiated transmission by 58dB. The circuit operates without an offset signal. Elements include digital phase detector with steering operating to 1.3GHz and digital frequency divider with programmable modulus from 1 to 1.5 in steps of 0.03125. Current is 10mA from 2.7V. Die is 1.2mm^2.

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K. Osada

11.1: Universal-Vdd 0.65-2.0V 32kB Cache using Voltage-Adapted Timing-Generation Scheme and a Lithographically-Symmetric Cell

Kenichi Osada, Jin-Uk Shin*, Masood Khan*, Yu-de Liou*, Karl Wang*, Kenichi Shoji, Kenichi Kuroda**, Shuji Ikeda**, and Koichiro Ishibashi**

Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo, Japan,
*Hitachi Semiconductor America Inc., San Jose, CA, USA
**Semiconductor & Integrated Circuits Group, Hitachi, Ltd., Tokyo, Japan

This 32kB cache design operates from 120MHz at 1.7mW and 0.65V to 1.04GHz at 530mW and 2.0V with a single internal supply using 0.18µm CMOS technology. The wide voltage operating range is achieved using a voltage-adapted timing-generation scheme with plural dummy cells and a lithographically-symmetric cell (LS-cell).

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H. Mattausch

11.2: An Architecture for Compact Associative Memories with deca-ns Nearest-Match Capability up to Large Distances

Hans Jürgen Mattausch, Takayuki Gyohten, Yoshihiro Soda, Tetsushi Koide[1]

Hiroshima University, Higashi-Hiroshima, Japan, [1]The University of Tokyo, Tokyo, Japan

Associative-memory architecture for Hamming-distance search, compact implementation, and short nearest-matches times up to large distances are proposed. The main ideas are fast analog word comparison and self-adaptive winner-line-up amplification. An implementation in a 0.6µm 2-poly 3-metal CMOS technology with 32 rows and 128 columns verifies the key concepts. Search time is <38ns.

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B. Wicht

11.3: SRAM Current-Sense Amplifier with Fully-Compensated Bit Line Multiplexer

Bernhard Wicht, Doris Schmitt-Landsiedel, Steffen Paul[1], Anthony Sanders[1]

Technical University of Munich, Germany, [1]Infineon Technologies AG, Munich, Germany

A current-sense amplifier that fully compensates the bit line multiplexer based on an improved feedback structure is implemented in a 512x24b 1.8V SRAM macro in 0.18µm CMOS. 0.5ns reduction of read access time is measured with 0.4% additional area.

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K. Kanda

11.4: Abnormal Leakage Suppression (ALS) Scheme for Low-Standby-Current SRAMs

Kouichi Kanda, Nguyen Duc Minh[1], Hiroshi Kawaguchi and Takayasu Sakurai

University of Tokyo, Tokyo, Japan, [1]Toshiba Corporation, Japan

Abnormal leakage suppression (ALS) repairs standby current errors in SRAMs. By introducing leakage sensors, shift registers and fuses, ALS senses 1μA abnormal leakage, isolates the memory cell from VDD lines and thus suppresses abnormal leakage current. A 64kb test SRAM demonstrates effectiveness. Area overhead is 7%.

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J. Hill

11.5: A 900MHz 2.25MB Cache with On-Chip CPU - Now In Cu SOI

J. Michael Hill, Jonathan Lachman

Hewlett-Packard Company, Fort Collins, CO

The 500MHz 1.5MB cache with 50% increased bit count is ported from a 0.25µm bulk technology to a 0.18µm SOI process with local interconnect. The SOI technology used presented significant design challenges to match the 80% frequency increase expected for the CPU.

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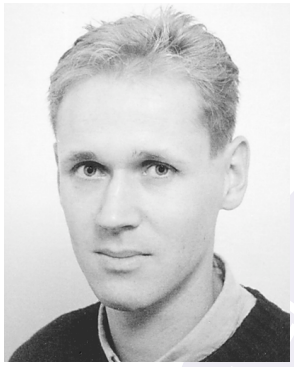

M. Bekooij

12.1: Power-Efficient Application-Specific VLIW Processor for Turbo Decoding

Marco Bekooij, John Dielissen, Françoise Harmsze, Sergej Sawitzki, Jos Huisken, Albert van der Werf, Jef van Meerbergen

Philips Research, Eindhoven, The Netherlands

A method permits coprocessors to be embedded inside a programmable VLIW processor. Synchronization of the coprocessors and the VLIW processor is determined at compile-time by the VLIW scheduler. The implementation of a power-efficient turbo decoder demonstrates effectiveness of this method.

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S. Gotoh

12.2: A Mixed-Signal 0.18µm CMOS SOC for DVD Systems with 432MSample/s PRML Read Channel and 16Mb Embedded DRAM

Shin-ichi Gotoh, Toshihiko Takahashi, Kozo Irie, Kazuya Ohshima, Nobuhiro Mimura, Kazutoshi Aida, Toshinori Maeda, Takashi Yamamoto, Koji Sushihara, Yoichi Okamoto, Yasuhiro Tai, Takeshi Nakajima, Makoto Usui, Takahiro Ochi, Katsuhiko Komichi, Akira Matsuzawa

Matsushita Electric Industrial Co. Ltd., Osaka, Japan

A single-chip CMOS mixed-signal LSI for DVD systems contains 32b RISC CPU, formatter, servo DSP, 16Mb DRAM, an ECC, ATA I/F, and digital read channel with 7b flash ADC. The chip in 0.18µm embedded DRAM process contains 24M transistors in a 144mm^2 die. The data rate is 432MSample/s with 1.2W power consumption.

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J. Chern

12.3: A 700Mb/s BiCMOS Read Channel Integrated Circuit

Shirish Altekar, Harry Chan, Jenn-Gang Chern, Richard Contreras, Leo Fang, Hairong Gao, Ralph Gee, Peter Ha, Kenny Hsieh, Yenyu Hsieh, David Hsu, Xi Huang, Howard Kim, Hiroshi Kimura, Paul Lai, Ishtiaque Mohammed, Larry Moser, Shih-Ming Shih, Mitsutoshi Sugawara[1],Yoshiyuki Tamura[1], Hemant Thapar, Yong Wang, Danfeng Xu, Jiazhi Yang, Alfred Yeung

LSI Logic, San Jose, CA, [1]NEC Electronics, Inc., Santa Clara, CA

A read channel IC achieves >1.5dB SNR improvement over a 32/34 rate EPRML read channel at 2.8 user bit density. The 0.18µm BiCMOS chip operates up to 700Mb/s with 1.8W read mode power using 3.3V analog and 1.8V digital power supplies. The die area is 9.64mm^2.

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D. Wei

12.4: A 300MHz Mixed-Signal FDTS/DFE Disk Read Channel in 0.6µm CMOS

Derrick Chunkai Wei[1], Daniel Q. Sun and Asad A. Abidi

Integrated Circuits & Systems Laboratory, University of California, Los Angeles, CA, [1]currently with Silicon Laboratories Inc., Austin, TX

A 300MHz mostly-analog DFE detector IC performs clock recovery and depth-of-two tree-search detection on equalized EPR4 waveforms. With MTR-coding, the detector is an analog DFE with digital error-correction logic to boost performance. At user density 3.0, performance exceeds that of an EPR4/VA channel. It consumes 530mW from 3V, and occupies 3.34mm^2 active area.

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H. Veenstra

12.5: A 1Gb/s Read/Write-Preamplifier for Hard-Disk-Drive Applications

Hugo Veenstra, Jan Mulder[1], Luan Le[2], Giuseppe Grillo

Philips Research, Eindhoven, The Netherlands

[1] Formerly with Philips Research, now with Broadcom, Bunnik, The Netherlands., [2] Philips Semiconductors, Caen, France.

The 6-channel read/write preamplifier IC supports data rates up to 1Gb/s. The bandwidth of the reader exceeds 630MHz. The input-referred noise is < 0.6nV/√Hz. The rise time of the writer is 0.3ns at 5mA output current. Impedance matching is employed at all high-frequency in/outputs. This IC uses 0.6µm CBiCMOS technology and occupies 16 mm^2.

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S. Rylov

12.6: A 2.3GSample/s 10-tap Digital FIR Filter for Magnetic Recording Read Channels

Sergey Rylov, Alexander Rylyakov, Jose Tierno, Michael Immediato, Michael Beakes, Mohit Kapur, Paul Ampadu[1], and Dale Pearson

IBM T.J. Watson Research Center, Yorktown Heights, NY,
[1]Cornell University, Ithaca, NY

A 6b 10tap 2.3GSample/s distributed-arithmetic digital FIR filter uses footless dynamic logic with delayed reset for precharge. The 0.5mm^2 filter, fabricated in 0.18µm CMOS, is operational from 1V to 2V power supply. At 2.3GSample/s, the power is 680mW, and at 1GSample/s the power is 120mW.

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J. van den Homberg

12.7: A 16b Accurate CMOS Laser Driver IC with 500mA Output Current and 1.5ns Rise Time

John van den Homberg[1], Andre Immink[1], Jamie McCormack[2], Andre Slenter[3], Jan Noot[2], Mischa Tryzna[4], Henri Verhoeven[4]

[1]Philips Research Laboratories, Eindhoven, The Netherlands
[2]Philips Optical Storage, Eindhoven, The Netherlands, [3]Philips Semiconductors, Eindhoven, The Netherlands, [4]Philips Consumer Electronics, Eindhoven, The Netherlands

A CMOS laser driver IC combines two 500MHz 250mA driver DACs with on-board digital write strategy generator and PLL to achieve 2ns timing resolution. An embedded laser power control algorithm with analog monitor diode pre-processing compensates for laser temperature variations and aging.

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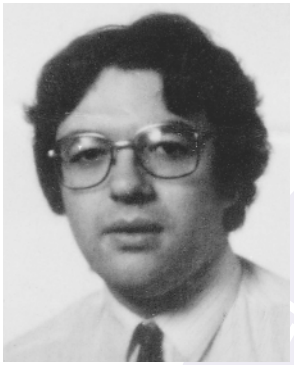

F. Op 't Eynde

13.1: A Fully-Integrated Single-Chip SOC for Bluetooth

Frank Op't Eynde[1], Jean-Jacques Schmit[1], Vincent Charlier[1], Rudolph Alexandre[1], Charles Sturman[2], Kevin Coffin[1], Bruno Mollekens[1], Jan Craninckx[1], Steven Terrijn[1], Andrea Monterastelli[1], Sofie Beerens[1], Paul Goetschalckx[1], Mark Ingels[1], Dieter Joos[1], Selim Guncer[3], Ared Pontioglu[3]

[1]Alcatel Microelectronics, Zaventem, Belgium, [2]TTP Communications, Melbourne, UK, [3]Alcatel Microelectronics Teletas, Istanbul, Turkey

A 0.25µm CMOS IC contains all analog and digital electronics required for a point-to-multipoint Bluetooth node. The circuit includes RF front-end and digital baseband processor, microprocessor and flash memory with software stack. The 41mm^2 die has 15dB noise figure and 2dBm maximum transmitter output, and consumes 125mW at 2.5V during receive.

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A. Ajjikuttira

13.2: A Fully-Integrated CMOS RFIC for Bluetooth Applications

Aruna Ajjikuttira, Chester Leung, Ee-Sze Khoo, Mark Choke, Rajinder Singh, Tian-Hwee Teo[1], Ban-Chuan Cheong[1], Jin-Hui See[1], Hwa-Seng Yap[1], Poh-Boon Leong[1], Choon-Tiong Law[1], Masaaki Itoh[1], Akira Yoshida[2], Yoshikazu Yoshida[2], Atushi Tamura[2] and Hiroshi Nakamura[2].

Institute of Microelectronics (IME), Singapore; [1]Oki Techno Center , Singapore (OTCS); [2]Oki Electric Industry, Hachioji, Tokyo, Japan.

A 4.5x4mm^2 single-chip Bluetooth RF transceiver in a 0.35µm standard CMOS technology with minimal external components operates from a 3V supply. The low-IF receiver achieves -77dBm sensitivity for 0.1%BER and -17dBm IIP3. The direct up-conversion transmitter has 0dBm nominal output power.

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H. Darabi

13.3: A 2.4GHz CMOS Transceiver for Bluetooth

H. Darabi, S. Khorram, E. Chien, M. Pan, S. Wu, S. Moloudi, J. C. Leete, J. J. Rael, M. Syed, R. Lee, B. Ibrahim, M. Rofougaran, A. Rofougaran

Broadcom Corp., El Segundo, CA

A fully-integrated CMOS transceiver tuned to 2.4GHz consumes 46mA in receive mode and 47mA in transmit mode from a 2.7V supply. The receiver has -80dBm sensitivity at 0.1% BER, and -7dBm IIP3. The transmitter delivers a GFSK modulated spectrum at 5dBm output power.

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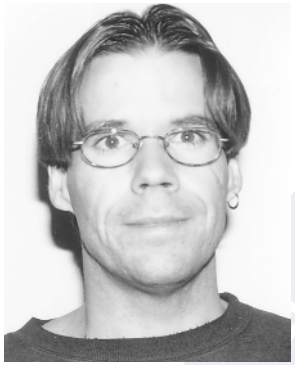

N. Filiol

13.4: A 22mW Bluetooth Transceiver with Direct RF Modulation and On-chip IF Filters

Norm Filiol, Neil Birkett, James Cherry, Florinel Balteanu, Christian Cojocaru, Ardeshir Namdar, Tolga Pamir, Kashif Sheikh, Gilles Glandon, Daniel Payer, Ashok Swaminathan, Robert Forbes, Thomas Riley[1], S.M. Alinoor, Edward Macrobbie, Mark Cloutier, Spyros Pipilos[2], Theo Varelas[2]

Conexant Systems Inc., Ottawa, Canada, [1]University of Oulu, Oulu, Finland, [2]Theta Microelectronics, Athens, Greece

A +2dBm Bluetooth transceiver in 0.5µm SiGe BiCMOS consumes 22mW at 2V. The transmitter uses a $\Delta\Sigma$ synthesizer and on-chip VCO to directly modulate the carrier and settles to 30ppm within 180µs. The single low-IF I/Q receiver uses a 7th-order complex IF filter with tuning, distributed AGC and digital PLL demodulation.

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P. Stroet

13.5: A Zero-IF Single-Chip Transceiver for up to 22Mb/s QPSK IEEE802.11b Wireless LAN

Peter M. Stroet, Rishi Mohindra, Steffen Hahn, Axel Schuur, Emmanuel Riou

Philips Semiconductors, Sunnyvale, CA

A zero-IF 2.4GHz 22Mb/s IEEE802.11b transceiver including LNA, mixers, on-chip channel filtering, fully-integrated VCO, AGC, RSSI and synthesizer is realized in a 0.5?m BiCMOS process. The receiver has 5.4dB NF, -4dBm IIP3, and dissipates <300mW. It delivers either 0 or 5dBm, and consumes <370mW at 3V.

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H. Komurasaki

13.6: A Single-Chip 2.4GHz RF Transceiver LSI with a Wide-Range FV Conversion Demodulator

Hiroshi Komurasaki, Hisayasu Sato, Masayoshi Ono, Takeo Ebana[1], Harunobu Takeda[1], Kohji Takahashi[1], Yutaka Hayashi, Tetsuya Iga, Kohichi Hasegawa, Takahiro Miki

Mitsubishi Electric Corp., Itami, Hyogo, Japan, [1]Mitsubishi Electric Engineering Company Limited, Sagamihara, Kanagawa, Japan

A single-chip RF transceiver LSI for 2.4GHz-band GFSK applications uses a 0.5µm BiCMOS which provides 23GHz f_T. The transceiver consumes 34.4mA in TX mode (PA, PLL) and 44.0mA in RX mode (LNA, IR mixer, filters, limiter, RSSI, demodulator, PLL). It has a linear FV conversion demodulator with wide input-frequency range.

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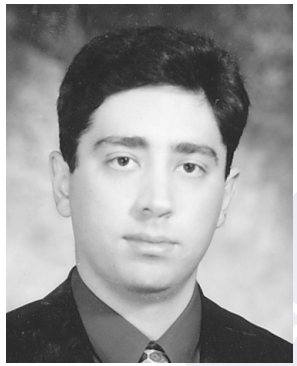

H. Samavati

13.7: A Fully-Integrated 5GHz CMOS Wireless-LAN Receiver

Hirad Samavati, Hamid R. Rategh, Thomas H. Lee

Stanford University, Stanford, CA

A fully-integrated 5GHz wireless LAN receiver in 0.24µm CMOS consumes 59mW and occupies 4mm^2 die space. The overall image rejection is 53dB and the noise figure is 7.2dB. IIP3 is -7dBm and LO leakage to the RF port is -87dBm. The synthesized LO phase noise is -134dBc/Hz at 22MHz and all spurs are below -70dBc.

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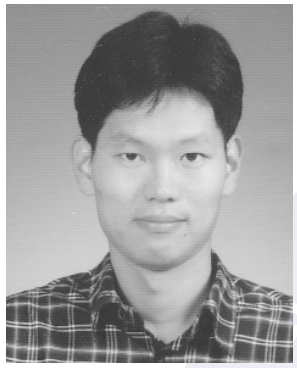

Y. Moon

14.1: A 0.6 - 2.5GBaud CMOS Tracked 3x Oversampling Transceiver with Dead-Zone Phase Detection for Robust Clock/Data Recovery

Yongsam Moon, Deog-Kyoon Jeong, and Gijung Ahn*

Seoul National University, Seoul, Korea, *Silicon Image, Sunnyvale, CA, U.S.A.

Tracked 3x oversampling with dead-zone phase detection is used in a receiver for robust clock/data recovery in the presence of excessive jitter and ISI. The transceiver, in 0.25µm CMOS, operates at 2.5GBaud over 10m 150Ω STP cable and at 1.25GBaud over 25m with $<10^{-13}$ BER.

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S. Anand

14.2: A 2.75Gb/s CMOS Clock-Recovery Circuit with Broad Capture Range

Seema Butala Anand, Behzad Razavi

University of California, Los Angeles

A dual-loop PLL clock-recovery circuit uses a digital search algorithm to increase capture range with no external reference. A 0.25µm CMOS circuit has 350MHz capture range around 2.7GHz, and 5.1ps rms jitter consuming 50mW from 2.7V.

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T. Nagahori

14.3: Si Bipolar Laser Driver/Receiver Chip Set for 4-Channel 5Gb/s Parallel Optical Interconnection

Takeshi Nagahori, Kazunori Miyoshi, Yukio Aizawa, Yuki Kusachi, Yasuaki Nukada, Nobuharu Kami

NEC Corp., Kawasaki, Japan

A chip set of a 4-channel 5Gb/s laser driver and a receiver uses an electo-optical mixed design with an array of laser diodes. It realizes a parallel optical transceiver module with 20Gb/s throughput. Optical waveform is not required. Power consumption is 1.3W.

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K. Phang

14.4: A 1V 1mW CMOS Front-End with On-chip Dynamic Gate Biasing for a 75Mb/s Optical Receiver

Khoman Phang, David A. Johns

Univ. of Toronto, Toronto, Ontario, Canada

An optical receiver front-end consisting of a transimpedance amplifier and two post amplifiers consumes 1mW from a 1V supply and provides 210kΩ transimpedance gain at 75Mb/s. A test chip in standard 0.35µm CMOS without low-threshold devices incorporates a charge pump for the biasing and tuning of MOS resistors.

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A. Tanabe

14.5: A Redundant Multi-Valued Logic for 10Gb/s CMOS Demultiplexer IC

Akira Tanabe, Yasushi Nakahara, Akio Furukawa, Tohru Mogami

NEC Corporation, Sagamihara, Kanagawa, Japan

A redundant multi-valued logic is used in >Gb/s communication IC applications. Using this logic, a quadruple data rate demultiplexer (serial-parallel converter) IC in 0.18µm CMOS achieves 10Gb/s operation with 1.3V supply and 38mW consumption.

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A. Brizio

14.6: A Chipset for Scalable QoS-Preserving Protocol-Independent Packet Switch Fabrics

Fabio Chiussi, Umesh Bakhru, Alberto Brizio, Garry Gu, Nasser Idirene, Khurram Kazi, Tao Li, John Leshchuk, Paul Moran, Declan Quinn, Alan Reynolds, Sheng Shen, Declan Staunton, Mohammad Syed, Thomas Wasilewski

Bell Labs, Lucent Technologies, Holmdel, NJ

The protocol independent switch fabric 128Gb/s provides per-flow quality of service (QoS) in the next-generation Internet. The VLSI challenges stem from the large number of QoS channels to be managed, the sophisticated scheduling algorithm used, and the need to relax chip synchronization requirements in systems.

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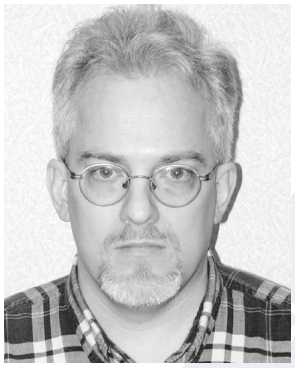

H. Wilson

14.7: A 28.5GB/s CMOS Non-Blocking Router for Terabit/s Connectivity between Multiple Processors and Peripheral I/O Nodes

Raj Nair, Nitin Y Borkar, Chris S. Browning, Gregory E Dermer, Vasantha Erraguntla, Venkatesh Govindarajulu, Amaresh Pangal, James D. Prijic, Linda Rankin, Erik Seligman, Sriram Vangal, Howard A. Wilson

Microprocessor Research Labs, Intel Corp., Hillsboro, OR, USA

A 28.5GB/s data router enables a terabits/s bandwidth network. The 6.6M transistor 0.18µm 1.3V 15W CMOS LSI has three clocking domains that synchronize data through four 1.06GB/s links, a 6-port crossbar, and five point-to-point links of 4.75GB/s data throughput each. Test data rates are up to 6.4Gb/s per wire.

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V. Pathak

14.8: 40Gb/s ASIC Switch Design Using Low-Jitter Clock Recovery

Vijay Pathak, Ching-Hao Shaw, Brad Vance, Srinath Devalapalli, Pat Smith, Andrea Bonelli[1], Jerome Ribo[1], Olivier Bonte[1], Francois Bauduin[1], Benoit Roderer[1], Manoj Verghese[2], Ian Grant[2], Harvey Mah[2], Carolyn Kean[2], Patrick Begin[2]

Texas Instruments, Dallas, TX, [1]Nice, France, [2]Nortel Networks, Ottawa, Ontario, Canada

A 32x32 switch ASIC has 40Gb/s aggregate throughput. The switch fabric is realized in three stages using full-custom clock recovery and transmit ports at 1.25Gb/s. 18 ASICs fabricated in 0.18µm CMOS technology and packaged in 352-pin flip-chip BGA dissipate 160W.

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L. Clark

15.1: A Scalable Performance 32b Microprocessor

Lawrence T. Clark, Eric Hoffman, Mark Schaecher, Manish Biyani, Dave Roberts, Yuyun Liao

Intel, Corp., Chandler, AZ

A RISC microprocessor core in a six-layer metal 0.18µm CMOS process implements the ARM™ V.5TE instruction set. The microprocessor core is 16.77mm^2 and dissipates 450mW at 1.3V, 600MHz, scaling between 55mW, 0.7V and 200MHz, and 1.55W at 1.65V and 800MHz.

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J. Petrovich

15.2: Physical Design of a Fourth-Generation POWER GHz Microprocessor

Carl J. Anderson, John Petrovick, John M. Keaty, James Warnock, Gary Nussbaum, Joel M. Tendler, Criag Carter, Sam Chu, Joachim Clabes, Jack DiLullo, Peter Dudley, Paul Harvey, Byron Krauter, John LeBlanc, Pong-Fei Lu, Bradley McCredie, Gerald Plum, Phillip J. Restle, Steve Runyon, Michael Scheuermann, Steve Schmidt, James Wagoner, Rick Weiss, Steve Weitzel, Brian Zoric

IBM Corp., Austin, TX

The 4th-generation POWER processor chip contains 170M transistors and includes 2 microprocessor cores, shared L2, directory for an off-chip L3, and all logic needed to interconnect multiple chips to form an SMP. It is implemented in a 0.18µm SOI technology, with 7 layers of Cu interconnect, and functions in systems at 1.1 GHz, and dissipates 115W at 1.5V.

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Y. Ho

15.3: A Process-Portable 64b Embedded Microprocessor with Graphics Extension and a 3.6GB/s Interface

Ying-wai Ho, Inder Bhasin, Tom Chiu, Per Forssell, Vincent Von Kaenel, James Jiang, John Kelley, Devon Matthews, Quaid Nasir, Ketan Patel, Victor Peng, Vidya Rajagopalan, Jim Reaves, Uttam Saha, George Tien, Kent Townley, Maria Ukanwa, Jeffrey Werner

MIPS Technologies Inc. Mountain View, CA

A custom yet process-portable dual-issue 64b embedded microprocessor implements the MIPS64™ architecture with 3D graphics geometry processing extensions and a 3.6GB/s interface. In a 0.18µm 6 layer metal process, the 34mm^2 processor is expected to function up to 600MHz, and dissipate 2W at 1.5V and 500MHz.

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A. Kowalczyk

15.4: First-Generation MAJC Dual Microprocessor

Andre Kowalczyk, Victor Adler, Chaim Amir, Frank Chiu, Choon Chng, Willem De Lange, Scott Dubler, Yuefei Ge, Subhendra Ghosh, Tan Hoang, Ray Hu, Baoqing Huang, Shree Kant, YS Kao, Cong Khieu, Suresh Kumar, Chung Lau, Lan Lee, Avi Liebermensch, Xin Liu, Naveen Malur, Hiep Ngo, Sung-Hun Oh, Ioannis Orginos, David Pini, Lorraine Shih, Balmiki Sur, Allan Tzeng, Dan Vo, Sanjay Zambare, Jin Zong

Sun Microsystems, Inc., Palo Alto, CA

The MAJC 5200 is a dual 32b microprocessor system-on-a-chip, utilizing 0.22µm CMOS with all-Cu interconnect. Two CPUs, delivering 6GFLOPS and 13GOPS at 500MHz, are tightly coupled through a shared, coherent, 4-way set associative 16kB data cache, and an on-chip 4GB/s switch. Each CPU is a 4-issue VLIW engine.

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B. Curran

15.5: A 1.1GHz First 64b Generation S/390 Microprocessor

Brian Curran, Peter Camporese, Sean Carey, Yuen Chan, Yiu-Hing Chan, Rainer Clemen[1], Rocco Crea, Dale Hoffman, Tim Koprowski, Mark Mayo, Tom McPherson, Greg Northrop[2], Leon Sigal[2], Howard Smith, Frank Tanzi, Patrick Williams

IBM Server Development, Poughkeepsie NY, [1]IBM Server Development, Boeblingen, Germany, [2]IBM Research Division, T.J. Watson Reaserch Center, Yorktown Heights, NY

The first 64b S/390 microprocessor implemented in a 0.18µm, 7-level copper interconnect bulk CMOS process, runs operating system and applications at 1.1GHz. The frequency is achieved with interconnect width and repeater optimization, selective use of low-Vt devices, tapered library gates, and improved synthesis and circuit tuning algorithms.

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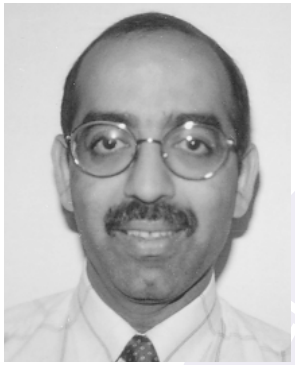

A. Jain

15.6: A 1.2GHz Alpha Microprocessor with 44.8GB/s Chip Pin Bandwidth

A. Jain, W. Anderson, T. Benninghoff, D. Bertucci, M. Braganza, J. Burnette, T. Chang, J. Eble, R. Faber, D. Gowda, J. Grodstein, G. Hess, J. Kowaleski, A. Kumar, B. Miller, R. Mueller, P. Paul, J. Pickholtz, S. Russell, M. Shen, T. Truex, A. Vardharajan , D. Xanthopoulos, T. Zou

Compaq Computer Corp., Shrewsbury, MA

A 4th-generation Alpha microprocessor running at 1.2GHz delivers up to 44.8GB/s chip pin bandwidth and dissipates 125W at 1.5V. It contains a 1.75MB 2nd level write-back-cache, two memory controllers supporting 8 Rambus™ channels running at 800Mb/s, four 6.4GB/s inter-processor communication ports, and a separate IO port capable of 6.4GB/s. The chip measures 21.1x18.8mm^2 and contains 130M transistors.

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E. Lauwers

16.1: A CMOS Multi-Parameter Biochemical Microsensor with Temperature Control and Signal Interfacing

Erik Y. Lauwers, Jan Suls, Geert Van der Plas, Erik Peeters, Walter Gumbrecht[1], David Maes[2], Filip Van Steenkiste[2], Georges G. Gielen, Willy M. Sansen

Katholieke Universiteit Leuven, Leuven, Belgium, [1]Siemens AG, Erlangen, Germany, [2]Imec, Heverlee, Belgium

A fully-integrated microsensor chip allows continuous monitoring of concentrations of blood gases (pH, pO_2, pCO_2), ions, and biomolecules, and a conductometric measurement. The chip monitors 7 different chemical properties and includes temperature control and an EPROM. It occupies 25.7mm^2 in a standard 1.2µm CMOS process including chemical sensor postprocessing.

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C. Hagleitner

16.2: A Single-Chip CMOS Resonant Beam Gas Sensor

Christoph Hagleitner, Dirk Lange, Oliver Brand, Andreas Hierlemann, Henry Baltes

Physical Electronics Laboratory, ETH Zurich, Zurich, Switzerland

A micromachined resonant beam gas sensor for detection of organic volatiles is monolithically integrated with thermal actuators, piezoresistive read out, and circuitry for self-excitation and fabricated in standard CMOS technology. Mass load due to analyte absorption in a sensitive coating changes beam resonance frequency. The limit of detection is 1ppm for toluene.

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J. Frounchi

16.3: Integrated Hall Sensor Array Microsystem

Javad Frounchi, Michel Demierre, Zoran Randjelovic, Rade S. Popovic

Swiss Federal Institute of Technology, Lausanne, Switzerland

A CMOS microsystem consists of an array of miniature integrated Hall sensors and dynamic offset cancellation interface electronics. It has 86V/Tesla magnetic sensitivity, 160µTesla magnetic offset field, and 0.8µTesla/√Hz noise density while consuming 2.3mA from a single 5V supply. It measures the earth magnetic field with 5% precision.

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R. Hashido

16.4: A Capacitive Fingerprint Sensor with Low-Temperature Poly-Si TFTs

R. Hashido, A. Suzuki, A. Iwata, T. Ogawa, T. Okamoto, Y. Satoh, M. Inoue

Advanced Technology R&D Center, Mitsubishi Electric Corp., Hyogo, Japan

A capacitive fingerprint sensor using low-temperature poly-Si TFTs succeeds in fingerprint certification. The array area is 19.2x15mm^2. Resolution is 423dpi (60µm pitch) using a structure with only one transistor and one sensor plate.

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R. Jeremias

16.5: A CMOS Photosensor Array for 3D Imaging Using Pulsed Laser

Ralf Jeremias, Werner Brockherde, Guenter Doemens[1], Bedrich Hosticka, Ludwig Listl[1], Peter Mengel[1]

Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany, [1] Siemens AG, Munich, Germany

A 32x2 pixel optical time of flight range sensor in standard 0.5µm CMOS acquires up to 20k 3D-images/s combines CDS, S&H, multiple double short time integration, a high-speed synchronous shutter, and a phase synchronizer enabling exposures <30ns with <5.2W/m^2 NEP. The 42mm^2 chip dissipates 330mW.

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J. Doutreloigne

16.6: A Versatile Micro-Power High-Voltage Flat Panel Display Driver

Jan Doutreloigne, Herbert De Smet, André Van Calster

University of Gent, ELIS-TFCG/IMEC, Belgium

A 0.7µm CMOS I²Technology display-driver chip with 100V driving capability and an internal power consumption of 1µW to 2µW per driver output is presented. These features together with its multi-functionality make this driver chip suited for a variety of flat-panel displays, especially in battery-powered applications.

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V. Brajovic

16.7: 100frames/s CMOS Range Image Sensor

Vladimir Brajovic, Kenichi Mori, Nebojsa Jankovic

The Robotics Institute, Carnegie Mellon University, Pittsburgh, PA

A row-parallel CMOS sensor for triangulation–based range imaging includes embedded winner-take-all circuits for detecting location of the brightest spot in each row. The brightest spot originates from a planar light continuously sweeping across a scene. The sensor delivers more than 100 range maps per second.

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L. McIlrath

17.1: Three-Dimensional Integrated Circuits for Low-Power High-Bandwidth Systems on a Chip

J. Burns[1], L. McIlrath[2], C. Keast[1], C. Lewis[2], A. Loomis[1], K. Warner[1], P. Wyatt[1]

[1]Lincoln Laboratory, MIT, Lexington, MA, [2]3D-IC, Lexington, MA

A 3D integration technology stacks two silicon circuit layers and connects them through unrestricted placement of 6µm square vias up to 7.5µm deep. A back-illuminated 64x64 active pixel sensor with fully-parallel A/D conversion is reported.

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M. Koyanagi

17.2: Neuromorphic Vision Chip Fabricated Using Three-Dimensional Integration Technology

Mitsumasa Koyanagi, Yoshihiro Nakagawa, Kang-Wook Lee[1], Tomonori Nakamura, Yuusuke Yamada, Kiyoshi Inamura, Ki-tae Park, Hiroyuki Kurino

Department of Machine Intelligence and Systems Engineering, Tohoku University, Sendai, Japan, [1]Japan Science and Technology Corp. (CREST)

A 3D micro-system mimics the human retina and visual cortex. The system uses 2.5µm square, 30µm deep vias to connect a photodiode array layer to a CMOS circuit layer below.

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S. Pierce

17.3: 3-D Assembly Interposer Technology for Next-Generation Integrated Systems

Kenji Ohsawa, Hiroshi Odaira, Masayuki Ohsawa, Shigeo Hirade, Tomoo Iijima, Stephen G. Pierce

North Corp., Tokyo, Japan

An interposer structure and manufacturing technique provides ultra-thin packages. The goal is a wiring layer characterized by one-fourth the thickness and five times the wiring density of conventional methods. It comprises a low-cost multi-layer copper wiring process, and enhanced speed through formation of a low dielectric constant material.

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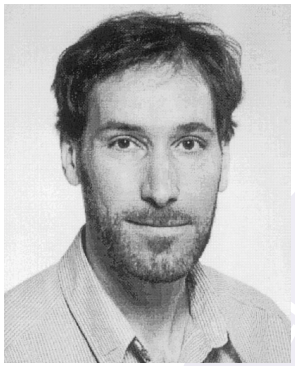

J. Long

17.4: Millimeter-Wave Characteristics of SiGe Heterojunction Bipolar Transistors and Monolithic Interconnects in Silicon Technologies

Jiaming Zhang, Michael K. Jackson, John R. Long[1], Saman Sadr[1]

ECE Dept., Vancouver, Canada, [1]ECE Dept., U. Toronto., Toronto, Canada

SiGe HBTs small-signal parameters are characterized to 150GHz using electro-optic sampling combined with on-wafer test fixtures. 300GHz measurement bandwidth is demonstrated for coplanar striplines in SiGe technology, validating 3-D simulations. Performance of coplanar and microstrip interconnects in SiGe and CMOS are compared up to 94GHz.

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S. Rusu

17.5: Backside Infrared Probing for Static Voltage Drop and Dynamic Timing Measurements

Stefan Rusu, Steve Seidel, Gary Woods, Dean Grannes, Harry Muljono, Jeremy Rowlette, Keiko Petrosky

Intel Corp., Santa Clara, CA

Infrared emission intensity and spectra are characterized for n-channel transistors from several process generations under both static bias and switching conditions using a HgCdTe detector array in the 0.9-1.45µm range. The infrared emission exponential dependence of voltage is used for accurate, non-invasive supply voltage drop and dynamic timing measurements in a microprocessor in 0.18µm technology.

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K. Bowman

17.6: Impact of Die-to-Die and Within-Die Parameter Fluctuations on the Maximum Clock Frequency Distribution

Keith A. Bowman, Steven G. Duvall[1], James D. Meindl

Georgia Institute of Technology, Atlanta, GA, [1]Intel Corp., Santa Clara, CA

A model for the maximum clock frequency (FMAX) distribution is derived and compared with wafer sort data for a microprocessor. Model predictions agree closely with measured data and reveal that intra-die fluctuations directly impact the FMAX mean. Inter-die fluctuations impact FMAX variance.

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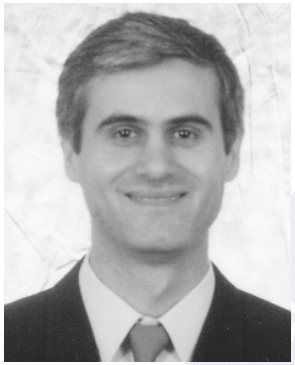

A. Naeemi

17.7: Sea of Leads: A Disruptive Paradigm for a System-on-a-Chip

Azad Naeemi, Chirag S. Patel, Muhannad S. Bakir, Payman Zarkesh-Ha, Kevin P. Martin, James D. Meindl

Georgia Institute of Technology, Atlanta, GA

Sea of leads (SoL) uses wafer-level batch fabrication of ultra-high-density (>10^4/cm^2) x-y-z compliant input/output leads and packages. Wafer-level DC/AC testing and burn-in to enhance performance, cost, size, weight, and reliability are assessed.

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J. Jussila

18.1: A 22mA 3.7dB NF Direct Conversion Receiver for 3G WCDMA

Jarkko Jussila, Jussi Ryynänen, Kalle Kivekäs, Lauri Sumanen, Aarno Pärssinen[1], Kari Halonen

Helsinki University of Technology, Helsinki, Finland, [1]Currently with Nokia Research Center, Helsinki, Finland

A single-chip 2GHz direct-conversion receiver including on-chip A/D converters achieving 3.7dB DSB NF and -16dBm IIP3 is targeted for third-generation WCDMA applications. The 10.3 mm^2 receiver IC is fabricated with 0.35µm 45GHz f_T SiGe BiCMOS technology and draws 22mA from a 2.7V supply.

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K. Lim

18.2: A Fully-Integrated CMOS RF Front-End with On-Chip VCO for WCDMA Applications

Kyoohyun Lim, Chan-Hong Park, Hyung Ki Ahn, Jae Joon Kim, Beomsup Kim[1]

Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea, [1]also at Stelsys Wireless Inc., San Jose, USA

A 0.35µm CMOS fully-integrated WCDMA RF front-end includes LNA, mixer, programmable gain amplifier, and ΣΔ modulated fractional-N synthesizer with on-chip VCO. Measured phase noise of the on-chip VCO is -134dBc/Hz at 1MHz offset. Sensitivity, DSB NF, IIP3, and maximum gain of the RF receiver are -107.9dBm, 3.5dB, -16dBm, and 80dB, respectively. Chip core area is 2mm^2 and DC power is 52mW at 3v.

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M. Ugajin

18.3: A 1V 12mW 2GHz Receiver with 49dB of Image Rejection in CMOS/SIMOX

Mamoru Ugajin, Junichi Kodate and Tsuneo Tsukahara

NTT Telecommunications Energy Labs, Atsugi, Kanagawa, Japan

A 2GHz receiver consisting of LNA, quadrature mixer, and on-chip polyphase filters achieves 49dB image rejection. The mixer employs an LC-tuned folded structure with a common RF input for I and Q channels, and suppresses phase errors in LO signals. The receiver IC is 2.2x3.8mm^2 and is fabricated in 0.2µm CMOS/SIMOX technology, dissipates 12mW at 1V, and provides 10dB NF with -15.7dBm IIP3.

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Z. Zhang

18.4: A 930MHz CMOS DC-Offset-Free Direct-Conversion 4-FSK Receiver

Zhaofeng Zhang, Zhiheng Chen, Louis Tsui, Jack Lau

Hong Kong University of Science & Technology, Hong Kong

A 0.35µm CMOS single-chip direct-conversion 4-FSK receiver including all necessary blocks eliminates both self-mixing and device mismatch induced DC offsets. The overall offset at the receiver output is <1mV. It consumes 58mW at 3V, occupies 4.6mm^2, has a 14.5dB NF with 10kHz IF, and -26dBm front-end IIP3.

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S. Tadjpour

18.5: A 900MHz Dual Conversion Low-IF GSM Receiver in 0.35µm CMOS

Shahrzad Tadjpour, Ellie Cijvat, Emad Hegazi, Asad Abidi

Electrical Engineering Department, University of California, Los Angeles

A low-power fully-integrated GSM receiver IC measuring 2.2x4mm^2 in 0.35µm CMOS uses a dual-conversion low-IF architecture with on-chip VCO and full channel selection, image suppression and more than 100dB of controllable gain. It consumes 24mA from a 2.5V power supply. The receiver has 5dB noise figure and -16dBm IIP3 .

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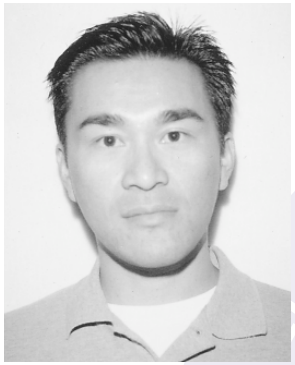

L. Der

18.6: A 2GHz CMOS Image-Reject Receiver with Sign-Sign LMS Calibration

Lawrence Der, Behzad Razavi

Electrical Engineering Department, University of California, Los Angeles, CA

A Weaver image-reject architecture incorporates an LMS algorithm to simultaneously calibrate gain and phase mismatches. In digital 0.25µm CMOS technology, the receiver achieves 57dB image-rejection ratio, 5.2dB noise figure, and -17dBm IIP3. The circuit consumes 50mW from a 2.5V supply and occupies 1.23x1.84mm^2.

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P. Laaser

19.1: A 285mW CMOS Single Chip Analog Front End for G.SHDSL

P. Laaser, T. Eichler, H. Wenske, D. Herbison, H. Eichfeld

Infineon Technologies AG, Munich, Germany

A 0.5µm CMOS single-chip analog front end for G.SHDSL consists of transmit current-steering DAC, noise shaping filter, on-chip line driver, receive ADC, multi-bit 3rd-order ΔΣ ADC and active hybrid for analog echo cancellation. The 12.8mm^2 AFE dissipates 285mW from 5V supply and supports 2.3Mb/s at 7.5kft.

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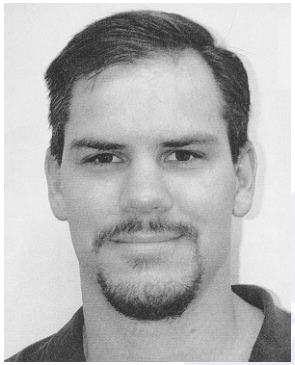

A. Krone

19.2: A CMOS Direct Access Arrangement using Digital Capacitive Isolation

Andrew Krone, Tyson Tuttle, Jeffrey Scott, Jerrell Hein, Timothy Dupuis, Navdeep Sooch

Silicon Laboratories, Inc., Austin, TX

0.5µm CMOS direct access arrangement (DAA) uses high-voltage discretes to interface device to the PSTN with loop current used for power source.

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R. Benton

19.3: A High-Voltage Line Driver for Combind Voice and ADSL Services

Roger Benton, Russell Apfel, Bruce Webb, Jerome Wenske, Walt Schopfer, Frank Thiel

Legerity, Inc., Austin TX

A 170V line driver allows voice and full-rate ADSL through a single line interface without splitters. Low noise and good THD support data rates up to 8Mb/s. The device is built in a high-voltage bipolar process and consumes <2W.

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M. Corsi

19.4: An ADSL Central Office AFE Integrating an Actively-Terminated Line Driver, Receiver, and Analog Filters

M. Corsi, R. Hester, K. Maclean, M. Agah, J. Quarfoot, C. Kozak, N. Gibson, T. Hagen

Texas Instruments, Dallas, TX

An analog front-end, fabricated in oxide-isolated complementary BiCMOS, integrates the analog filters, synthesized-impedance line driver, and receiver amplifier required for FDD ADSL central office applications. External passives allow flexibility in hybrid design. The device employs a single 15V supply and dissipates 1.1W.

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T. Piessens

19.5: SOPA: A Highly-Efficient Line Driver in 0.35µm CMOS Using a Self-Oscillating Power Amplifier

Tim Piessens, Michiel Steyaert

Katholieke Universiteit Leuven, Heverlee, Belgium

A driver in mainstream digital 0.35µm 3.3V technology drives loads down to 2.4Ω with efficiency >61% and 56.4dB spurious-free dynamic range. It uses a self-oscillating scheme and coupling 2 self-oscillating power amplifiers with a transformer. The chip occupies 4.6mm^2.

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R. He

19.6: A DSP Based Receiver for 1000BASE-T PHY

Runsheng He, Nersi Nazari, Sehat Sutardja

Marvell Semiconductor, Inc. Sunnyvale, CA

The receiver architecture of a CMOS IC that implements 1000BASE-T PHY achieves 1000Mb/s transmission over 4-pair Cat-5 cabling up to 17m. The DSP based receiver incorporates echo&NEXT cancellers, decision feedback sequence estimator, timing recovery, baseline wander and delay skew compensation. The power consumption is 1.8W.

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P. Roo

19.7: A CMOS Transceiver Analog Front-end for Gigabit Ethernet over CAT-5 Cables

Pierte Roo, Sehat Sutardja, Shuran Wei, Farbod Aram, Yi Cheng

Marvell Semiconductor, Inc., Sunnyvale, CA

An integrated transceiver for gigabit Ethernet over UTP CAT-5 cables uses 0.18µm CMOS. The mixed-signal processing circuits use analog echo cancellation and baseline correction with extensive DSP to achieve a maximum transmit distance of 170m (BER<10^{-10}). Dissipation is 1.8W on-chip using a single 3.3V supply. The die is<25mm^2.

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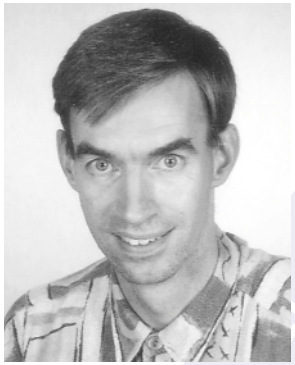

J. Leenstra

20.1: A 1.8GHz Instruction Window Buffer

Jens Leenstra, Juergen Pille, Antje Mueller, Wolfram Sauer, Rolf Sautter, Dieter Wendel

IBM Entwicklung GmbH, Boeblingen, Germany

An instruction window buffer implements the processor parts for renaming, reservation station and reorder buffer as a 64-entry unified buffer. Using 0.18µm 1.5V CMOS, it supports operation up to 1.8GHz. This frequency is enabled by port reduction techniques, the instruction issue structure, and the use of self-resetting circuits.

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A. Inoue

20.2: A Low-Power SOI Adder Using Reduced-Swing Charge-Recycling Circuits

Atsuki Inoue[1], Vojin G. Oklobdzija[2], William W. Walker[1], Mutsuaki Kai[3], Tetsuo Izawa[3]

[1]Fujitsu Laboratories of America, Inc., Sunnyvale, CA, [2]Integration Corp., Berkeley, CA, [3]Fujitsu Limited, Kanagawa, Japan

A low-power clocked static low-swing charge-recycling circuit technique is applied to a 32b carry skip adder and fabricated in 0.08µm SOI CMOS. Power consumption is reduced by 50% with no speed degradation compared to that of a conventional CMOS adder.

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S. Mathew

20.3: Sub-500ps 64b ALUs in 0.18µ SOI/Bulk CMOS: Design & Scaling Trends

Sanu Mathew, Ram Krishnamurthy, Mark Anders, Rafael Rios, Kaizad Mistry, K. Soumyanath

Intel Corp., Hillsboro, OR

A 482ps 64b Han-Carlson ALU in 1.5V 0.18µm bulk CMOS directly ported to 0.18µm SOI offers 14% performance improvement, after a 2% margin is added for reverse body effect. An SOI-optimal redesign using a quaternary-tree architecture improves the speedup to 19%. Scaling the designs to 0.13µm for the two cases results in overall speedup of 9% and 16%, respectively.

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R. Hokinson

20.4: Design and Migration Challenges for an Alpha Microprocessor in a 0.18µm Copper Process

Raymond Hokinson, Bradley Benschneider, Mikael Arneborn, Don Clay, John Clouser, Scott Dumford, Venkat Kalathur, Varma Kalidindi, Suma Kovvali, Jon Krause, Stephen Maresh, Ben Munger, Niall O'Neill, Ilan Pragaspathy, Wendy Qin, Russell Sasamori, Steve Sayadi, Tejpal Singh, Jinjie Tang, Matt Tracz, Steve Watkins

Compaq Computer Corp., Shrewsbury MA

An Alpha microprocessor with clock frequency >1.3 GHz is achieved by migrating to a 0.18µm CMOS process with 7 layers of copper interconnect. The technology challenges of converting an aluminum-based design to copper are presented. The circuit and design solutions introduced by the technology are discussed.

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L. Tsai

20.5: A 1GHz PA-RISC Processor

Li C. Tsai

Hewlett Packard Company, Fort Collins, Colorado

The processor is a leveraged design based on a previous generation of PA-RISC processor. Improvements over the previous design are: a 0.18µm silicon-on-insulator (SOI) process with 7-layer metal interconnects, 2.25MB cache with row and column redundancies, 120-entry TLB, 50% frequency boost, and 45% lower power with the same footprint.

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D. Sager

20.6: A 0.18µm CMOS IA Microprocessor with a 4GHz Integer Execution Unit

David Sager, Glenn Hinton, Michael Upton, Terry Chappell, Thomas D. Fletcher, Samie Samaan, Robert Murray

Intel Corp., Hillsboro, OR

A microprocessor with an integer execution unit capable of fully-dependent operations at 4GHz is fabricated in 0.18µm CMOS with 6 Al layers. Micro-architectural and circuit techniques used are described.

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L. D'Luna

21.1: A Universal Cable Set-Top Box System on a Chip

Lionel D'Luna, Hon-Man Law, Joe Laskowski, William Ngai, Tzu-Chieh Kuo, Jeffrey Tang, Xiaodong Xie, James Patterson, Young Vu, Carolyn Walker, Francis Cheung, Cam Luu, Michael Case, Jim Anderson, Frank Gomez, Larry Osborne, Stephen Jantzi, Darwin Cheung, Ardie Venes, Paige Bushner, Jeff Echtenkamp, David Bogosh, Henry Samueli

Broadcom Corp., Irvine, CA.

The device integrates a complete digital cable TV transceiver, MPEG-2 audio and video decoder, 2-D/3-D graphics processor and CPU running at 81MHz to achieve a true set-top box system-on-a-chip. The 14.6M transistor IC in a 0.22µm CMOS process, consumes 3W, and incorporates all required A/Ds and D/As for QAM/QPSK, audio, and video.

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J. Goodman

21.2: An Energy-Efficient IEEE 1363-based Reconfigurable Public-Key Cryptography Processor

James Goodman[1], Anantha P. Chandrakasan[2]

[1]Chrysalis-ITS, Ottawa, Canada, [2]Massachusetts Institute of Technology, Cambridge, MA

A reconfigurable public-key cryptography processor has 2 to 3 orders of magnitude lower energy consumption than existing software and programmable logic-based implementations. The processor ISA is based on the IEEE 1363-2000 Public Key Cryptography Standard. At 50MHz the processor consumes 75mW at 2V V_{DD} in 0.25µm CMOS. At 3MHz it consumes 525µW at 0.7V.

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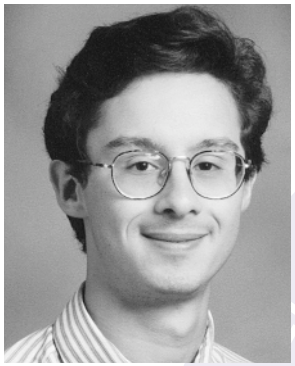

E. Grayver

21.3: A Self-Contained 100µW Multirate FSK Receiver ASIC

Eugene Grayver, Babak Daneshrad

UCLA Electrical Engineering Dept., Los Angeles, CA

A self-contained FSK receiver targets deep-space and terrestrial communications. It supports variable data rates and is robust against Doppler. Key features are subsampling, 1b quantization, and FFT based detection. Low-power circuits are designed for FFT, DDFS, and decimation. The power consumption is below 100µW for data rates below 20kbps. Rates up to 2Mb/s are supported.

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H. Ohwada

21.4: A Single-chip Band-Segmented-Transmission OFDM Demodulator for Digital Terrestrial Television Broadcasting

Hideo Ohwada, Masahiro Yoshida, Nobuaki Ohtaka, Makoto Hamaminato, Koichi Hatta*, Masaya Tamamura*, Yukio Otobe

Fujitsu Labs, Kawasaki, Kanagawa, Japan, *Fujitsu Ltd.

A single-chip OFDM demodulator for Japanese Digital Terrestrial TV integrates all necessary OFDM demodulator functions, such as 10b ADC, 8192-point FFT processor, and error correction. The chip has multi-layer transport stream capability for a variety of services relevant to future digital broadcasting.

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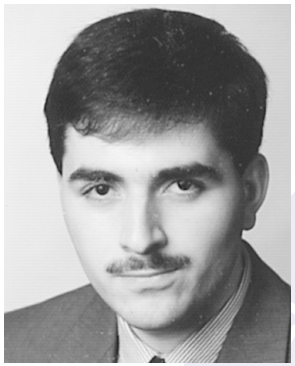

W. Eberle

21.5: A Digital 72Mb/s 64-QAM OFDM Transceiver for 5GHz Wireless LAN in 0.18µm CMOS

Wolfgang Eberle[1], Veerle Derudder, Liesbet Van der Perre, Geert Vanwijnsberghe, Mario Vergara, Luc Deneire, Bert Gyselinckx, Marc Engels, Ivo Bolsens, Hugo De Man[2]

IMEC, Leuven, Belgium, [1]also PhD Student at KU Leuven, [2]also Professor at KU Leuven

A parameterizable 64-carrier OFDM transceiver for 72Mb/s 5GHz wireless LAN with a 20MHz bandwidth encompasses (de)framing, (I)FFT, adaptive interpolating equalization for BPSK, QPSK, 16-QAM and 64-QAM, full synchronization and tracking. The 20.8mm^2 0.18µm 1.8V/3.3V CMOS IC, based on distributed control and dynamic clock gating, uses a mixed C++/VHDL flow.

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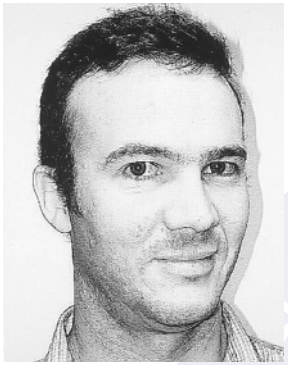

P. Ryan

21.6: A Single Chip PHY COFDM Modem for IEEE 802.11a with integrated ADCs and DACs

Philip Ryan, Thangadurai Arivoli, Ludovico de Souza, Gordon Foyster, Richard Keaney, Tom McDermott, Alireza Moini, Said Al-Sarawi, Uri Parker, Geoff Smith, Neil Weste, Greg Zyner

Radiata Communications, North Ryde, NSW, Australia

A single-chip 64 tone OFDM modem that provides for 6 to 54Mbs WLANs is implemented in 0.25µm 5M-1P CMOS. The 3.7M transistor mixed-signal chip contains a fully compliant 802.11a modem, dual 10b 40MHz ADCs, dual 10b 80MHz DACs, and a 5b RSSI ADC.

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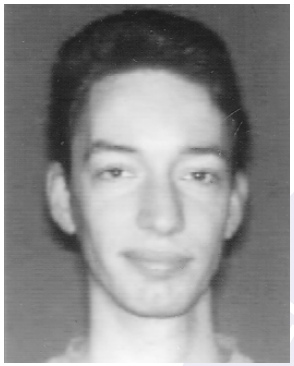

M. van Heijningen

22.1: Substrate Noise Generation in Complex Digital Systems: Efficient Modeling and Simulation Methodology and Experimental Verification

Marc van Heijningen, Mustafa Badaroglu[1], Stephane Donnay, Hugo De Man, Georges Gielen[2], Marc Engels, Ivo Bolsens

IMEC, Leuven, Belgium. [1] Also Ph.D student at K.U. Leuven. [2] K.U. Leuven, Belgium.

An 86kgate ASIC has on-chip noise sensors for accurate direct substrate noise measurements. Modeling and simulation methodology accurately predict substrate noise generation of large digital circuits. The difference between measured and simulated RMS substrate voltage is <10%.

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H. Mizuno

22.2: ChipOS: Open Power-Management Platform to Overcome the Power Crisis in Future LSIs

Hiroyuki Mizuno and Takayuki Kawahara

Central Research Lab, Hitachi, Ltd., Tokyo, Japan

ChipOS, a power-aware operating system in a chip, provides open power-management platform for system-on-a-chip devices. It enables a large degree of high-speed operation on a limited power budget in the same way that operating systems now make personal computers run multiple applications with a limited computing or memory capacity.

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M. Mizuno

22.3: Elastic Interconnects: Repeater-Inserted Long Wiring Capable of Compressing and Decompressing Data

Masayuki Mizuno, [1]William J. Dally, and Hideaki Onishi

NEC Corporation, Kanagawa, Japan, [1]Stanford University, Stanford, CA

A network communication technique, elastic interconnect, is made possible using on-chip repeater-inserted long wiring. Latency, throughput, and saturation throughput are improved by approximately 20% to 40% in simulations by compressing and decompressing data in interconnects.

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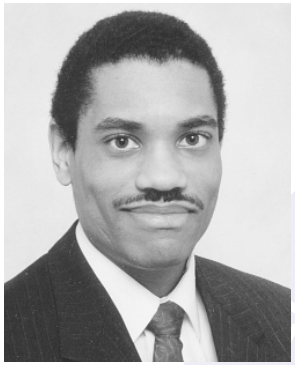

J. Williams

22.4: An Implementation of Two Multiprocessor DSPs: A Design Methodology Case Study

Joseph Williams, Jay O'Neill

Lucent Technologies, Holmdel, NJ

Implementation results of two code-compatible multiprocessor DSPs are presented. Although process, libraries, and tools where identical, one design achieved 16x the peak DSP MIPS of the other in the same die area. Transistor density improved by 10x and clock frequency by 2x. Results demonstrate the impact of design methodology on IC design.

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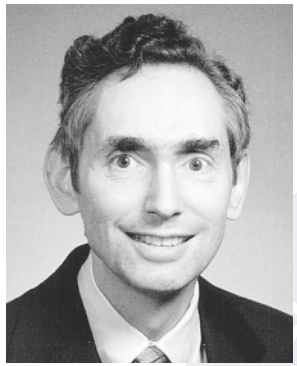

R. Walden

22.5: A GSM 2+ Conversion Signal Processor forContinuous Full-Duplex EDGE/GPRS Applications

Robert W. Walden, Ramin Khoini-Poorfard*, H. Scott Fetterman, Thomas Hearn, Roger M. Jeffery, Peter Liu, Arthur Lukoff***, Mandell Mangahas, David G. Martin, Jose G. Mena, Andrew L. Webb**

Lucent Techonologies, Allentown, PA, *Silicon Labs, Allentown, PA, **Optronx Inc., Allentown, PA, ***PMC-Sierra, Allentown, PA

A 35mm^2 0.3µm 3V CMOS IC supports both continuous and full-duplex classes of EGPRS / GSM 2+ operation with reduced standby power. The chip includes digital offset correction, actively-tuned baseband filters, an expanded GSM-optimized programmable timing control unit, and a power-saving ADC architecture.

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T. Delmot

22.6: A Fully-Configurable GSM BTS Controller and GMSK-EDGE Base-Band Transmitter IC

Thierry Delmot, Emanuel Marreel, Frans Bonjean, Bart Verstraeten, Silvio Taraborrelli, Anders Udahl[1], Geir Åge Noven[1], Rüdiger Bauernschmitt[2], Peter Brendle[2], Rolf Nüchter[2], Bernd Herold[2], Thomas Schütz[2], Ralf Walter[2]

ASIC Design Department, Alcatel Telecom Belgium, Antwerp, Belgium. [1]Alcatel Telecom Norway, Oslo, Norway. [2]Alcatel Telecom Germany, Stuttgart, Germany.

A GSM base transceiver station controller and base band transmitter in a CMOS 0.5µm 3.3V technology embeds a fully-configurable GMSK/EDGE baseband signal generator, a power-ramping controller, and a dual fully-programmable 10 to 270MHz PLL. One bandgap reference voltage and four programmable calibration voltage generators are also integrated.

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J. Vankka

22.7: A Multicarrier GMSK Modulator for Base Stations

Jouko Vankka, Jaakko Pyykönen[1], Johan Sommarek, Mauri Honkanen[1], Kari Halonen

Helsinki University of Technology, Espoo, Finland, [1]Nokia Research Center, Finland

A multicarrier GMSK modulator with 14b on-chip D/A converter occupies 26.8mm^2 in 0.35µm CMOS (in BiCMOS) and dissipates 706mW at 3.3V with 52MHz. Power ramping and dynamic output power level control is digital. The digital modulator fulfills spectrum and phase error specifications of GSM 900 and DCS 1800 base stations.

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Marcus May

23.1: A Synchronous Dual-Output Switching dc-dc Converter Using Multibit Noise-Shaped Switch

Marcus W. May, Michael R. May, John E. Willis

Sigmatel Corp., Austin, TX

A synchronous dc-dc converter generates two indepedent output voltages using a single external inductor. The all-digital control logic includes a multibit ΣΔ modulator, which reduces quantization artifacts from synchronous switching of the inductor. The circuit occupies 0.6mm^2, consumes 3.5mW, and reaches efficiencies >80%.

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N. Krishnapura

23.2: Dynamically Biased 1MHz Low-pass Filter with 61dB peak SNR and 112dB Input Range

Nagendra Krishnapura, Yannis Tsividis

Columbia University, New York, NY

In quiescent condition, a dynamically biased filter, occupying 0.52mm^2 in a 0.25µm BiCMOS process, draws 575µW from 2.5V, and has 4.4nA rms output noise. S/N is >50dB over 3 decades of input and THD is <1% for inputs <2.5mA peak. The bias can be varied to minimize noise and power consumption without disturbing the output.

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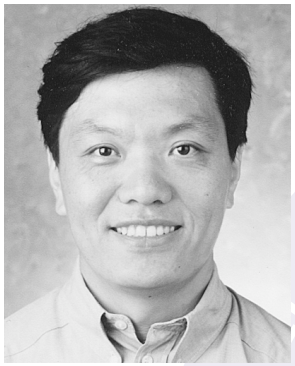

Q. Huang

23.3: A 200nV Offset 6.5nV/√Hz Noise PSD 5.6kHz Chopper Instrumentation Amplifier in 1µm Digital CMOS

Qiuting Huang, Christian Menolfi

Integrated Systems Laboratory, ETH Zurich

Simple clocking substantially reduces residual offset usually found in chopper amplifiers due to charge injection. Compared to well-established techniques of using LP or BP amplifiers for residual offset reduction, improvement is 5-fold over state-of-the-art. Bandwidth is not sacrificed, so chopper frequency is 350x that used in the nested chopper technique. Noise psd is as low as 6.5nV/√Hz and CMRR is 150dB.

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E. Hegazi

23.4: A Filtering Technique to Lower Oscillator Phase Noise

Emad Hegazi, Henrik Sjöland, Asad Abidi

Electrical Engineering Department, University of California, Los Angeles, CA

A filtering technique reduces phase noise of differential LC oscillators using passive LC filters. Three fully-integrated LC VCOs serve as proof of concept. Two 1GHz VCOs achieve -152dBc/Hz and -148.5dBc/Hz at 3MHz offset, biased at 3.7mA from 2.5V. A 2.1GHz VCO achieves -148dBc/Hz at 15MHz offset, drawing 4mA from 2.7V supply.

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A. Van den Bosch

23.5: A 12b 500MSample/s Current-Steering CMOS D/A Converter

Anne Van den Bosch, Marc Borremans, Michiel Steyaert, Willy Sansen

Katholieke Universiteit Leuven. Belgium

A 12b 500MSample/s current-steering CMOS DAC requires no tuning or trimming. INL is 0.3LSB. SFDR is 74.3dB at 500kHz and 62dB at 125MHz for an update rate of 500MSample/s. At this update rate, the DAC consumes 110mW for a Nyquist output signal. The chip has 1mm^2 active area.

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D. Li

23.6: A 1.9GHz Si Active LC Filter with On-Chip Automatic Tuning

Dandan Li[1], Yannis Tsividis[2]

[1]Lucent Technologies, Murray Hill, NJ, [2]Columbia University, New York, NY

A 1.9GHz 4th-order bandpass active LC filter, which exhibits 49dB SFDR and 1dB compression DR of 63dB, is integrated in 0.25µm resonator BiCMOS. An on-chip tuning system automatically adjusts center frequency Q. The filter draws 18mA from a 3V supply, with another 18mA drawn periodically while the tuning mechanism is activated.

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C. De Ranter

23.7: A 0.25µm CMOS 17GHz VCO

Carl R. C. De Ranter, Michiel S. J. Steyaert

ESAT-MICAS, KULeuven, Leuven, Belgium

A 17GHz fully-integrated VCO uses global optimization of all blocks. Layout is symmetrical. Measurements show a phase noise as low as -108dBc/Hz at 1MHz for a 10.5mW power consumption. The tuning range is 8.6%. A 0.25µm 4-metal standard CMOS technology is used.

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H. Wang

23.8: A 50GHz VCO in 0.25µm CMOS

HongMo Wang

Bell Labs, Murray Hill, NJ

A fully integrated 50GHz VCO in 0.25µm CMOS works with a 1.3V supply and consumes 13mW. The measured phase noise is -99dBc/Hz at 1MHz offset from the center frequency and the tuning range is 1.1GHz.

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J. Kucera

23.9: A Wideband BiCMOS VCO for GSM/UMTS Direct Conversion Receivers

Jakub J. Kucera

Infineon Technologies Wireless Products, Munich, Germany

A packaged 1.75-2.51GHz VCO has phase noise of -99dBc/Hz and -128.5dBc/Hz at 20kHz and 600kHz frequency offset, respectively. The differential VCO in 25GHz BiCMOS technology dissipates 12mW and uses the package bond-wire of a standard TSSOP plastic package with an on-chip pn diode as resonator.

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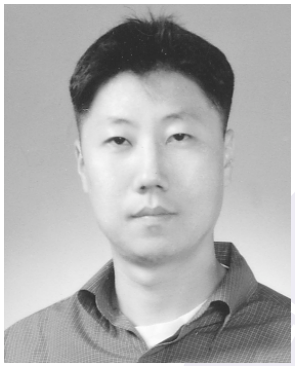

H. Yoon

24.1: A 4Gb DDR SDRAM with Gain-Controlled Pre-Sensing and Reference Bitline Calibration Schemes in the Twisted Open Bitline Architecture

Hongil Yoon, Jae Yoon Sim, Hyun Suk Lee, Kyu Nam Lim, Jae Young Lee, Nam Jong Kim, Keum Yong Kim, Sang Man Byun, Won Suk Yang, Chang Hyun Choi, Hong Sik Jeong, Jei Hwan Yoo, Dong Il Seo, Kinam Kim, Byung Il Ryu, and Chang Gyu Hwang

Samsung, Kyungki, Korea

A 1.8V 645mm^2 4Gb DDR SDRAM provides low-voltage high-speed operation at full density. Inter-bitline coupling noise is reduced in the twisted open bitline architecture. The amplifier sensitivity and sensing margin are improved with gain-controlled pre-sensing and active calibration of the bitline precharge voltage.

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T. Takahashi

24.2: A Multi-Gigabit DRAM Technology with 6F^2 Open Bit-line Cell Distributed Over-Driven Sensing and Stacked-Flash Fuse

Tsugio Takahashi, Tomonori Sekiguchi1, Riichiro Takemura[1], Seiji Narui, Hiroki Fujisawa, Shinichi Miyatake[2], Makoto Morino[2], Koji Arai[2], Satoru Yamada, Shoji Shukuri[3], Masayuki Nakamura, Yoshitaka Tadaki, Kazuhiko Kajigaya, Katsutaka Kimura[1], and Kiyoo Itoh[1]

ELPIDA Memory, Inc., Kanagawa, Japan, [1]Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, [2]Hitachi ULSI Systems Co., Ltd., Tokyo, Japan, [3]Semiconductor & Integrated Circuits Div., Hitachi, Ltd., Tokyo, Japan

A multi-gigabit DRAM technology features a low-impedance array for 6F^2 open-bit-line cell, distributed overdriven sensing for operation below 1V, and stacked-flash fuse leading to a 10-order of magnitude fuse failure rate reduction. The technology, which can be used to fabricate a 0.13µm, 180mm^2 1GbDRAM, is verified using a 57.6 mm^2 200MHz array-cycle 256Mb test chip with 0.109µm^2 cells.

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T. Kirihata

24.3: A 113mm² 600Mb/s/pin 512Mb DDR2 SDRAM with Vertically Folded Bitline Architecture

Toshiaki Kirihata[1], Gerhard Mueller[2], Michael Clinton[1], Steffen Loeffler[2],Brian Ji[1], Hartmud Terletzki[2], David Hanson[1], Chorng-Lii Hwang[1],Gunther Lehmann[2], Daniel Storaska[1], Gabriel Daniel[2], Louis Hsu[1], Oliver Weinfurtner[2],Thomas Boehler[2], Josef Schnell[2], Gerd Frankowsky[2], Dmitry Netis1,John Ross1, Armin Reith[2], Oliver Kiehl[2], and Matthew Wordeman[1]

[1]IBM Microelectronics, Semiconductor R&D Center, Hopewell Junction, NY [2]Infineon Technologies, Hopewell Junction, NY

A 113mm² 512Mb DDR2 SDRAM employs a 4 quadrant architecture using a vertically folded bitline sensing and hierarchical row and column decoders for 6.6F² cross point vertical access gate cells. The chip supports 4b prefetch, back-to-back RAS, and flexible calibration, resulting in 600Mb/sec/pin.

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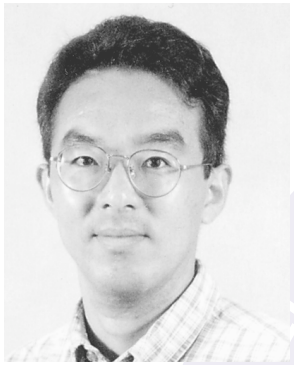

S. Tomishima

24.4: A 1.0V 230MHz Column Access Embedded DRAM Macro with Dual Interface and Triple Test Functions for Portable MPEG Applications

Shigeki Tomishima[1], Takaharu Tsuji[1], Toshiaki Kawasaki[2], Masatoshi Ishikawa[1], Toshihiro Inokuchi[2], Hiroshi Kato[1], Hiroaki Tanizaki[3], Wataru Abe[2], Akinori Shibayama[2], Yoshifumi Fukushima[2], Mitsutaka Niiro[1], Masanao Maruta[1], Toshitaka Uchikoba[2], Manabu Senoh[2], Shouji Sakamoto[2], Tsukasa Ooishi[1], Hirohito Kikukawa[2], Hideto Hidaka[1] and Kazunari Takahashi[2]

[1]Mitsubishi Electric Corp., Itami, Hyogo, Japan, [2]Matsushita Electric Industrial Co., Ltd., Nagaokakyo, Kyoto, Japan, [3]Mitsubishi Electric Engineering Co., Ltd., Itami, Hyogo, Japan

A 1.0V 230MHz random column access 32Mb embedded DRAM macro for portable MPEG codec LSI uses 0.13µm 3-well 4-level Cu embedded DRAM technology. Peak power consumption is suppressed to 198mW in burst accesses. With dual interface and triple test functions, the macro die is 18.9mm^2.

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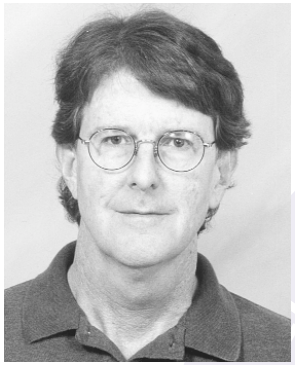

K. Hardee

24.5: A 1.43GHz Per Data I/O 16Mb DDR Low-Power Embedded DRAM Macro for A 3D Graphics Engine

Kim Hardee, O. Fred Jones, Michael Parris, Doug Butler, Larry Aldrich, Penny Austin, Ken Jacobsen, Masayuki Miyabayashi[1], Kazuo Taniguchi[1], Tomofumi Arakawa[1]

United Memories, Inc., Colorado Springs, CO, [1]Sony Corporation Semiconductor Network Co., Tokyo, Japan

A 15.75mm^2 16Mb embedded DRAM macro has 256 DDR I/Os and employs a hidden write function and local read/write data drivers to achieve 1.43GHz data rate with concurrent read/write for use in a 4Tera-b/s 3D graphics chip. The macro is fabricated in 1.5V 0.18µm CMOS.

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N. Watanabe

24.6: An Embedded DRAM Hybrid Macro with Auto Signal Management and Enhanced On-Chip Tester

Naoya Watanabe, Fukashi Morishita, Yasuhiko Taito, Akira Yamazaki, Tetsushi Tanizaki, Katsumi Dosaka, Yoshikazu Morooka, Futoshi Igaue[1], Katsuya Furue, Yoshihiro Nagura, Tatsuya Komoike, Toshinori Morihara, Atsushi Hachisuka, Kazutami Arimoto, Hideyuki Ozaki

Mitsubishi Electric Corp., Itami, Hyogo, Japan, [1]Mitsubishi Electric Engineering Co., Ltd., Itami, Hyogo, Japan

An embedded DRAM hybrid (hardware, software) macro generates a variety of memory specifications. The macro employs auto signal management providing more than 120k eDRAM macros and a range operation from 1.2 to 1.8V. An enhanced-on-chip tester realizes simultaneous 512b I/O repair analysis, and reduces the testing time to 1/64 that of conventional on-chip tester.

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J. Ingino

25.1: A 4GHz 40dB PSRR PLL for SOC Application

Joseph M. Ingino

SiByte Inc., Santa Clara, CA

A 4GHZ PLL employs a voltage regulator to achieve 40dB minimum PSRR using a gain boosted regulator. Peak cycle-to-cycle jitter is 25ps at 700MHz with a 500mV step on the regulator 3.3V supply. In a 0.15µm 5-metal digital CMOS process, area is 1.48mm^2, and power dissipation is 130mW.

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A. Maxim

25.2: A Low-Jitter 125-1250MHz Process-Independent 0.18µm CMOS PLL Based on a Sample-Reset Loop Filter

Adrian Maxim, Baker Scott, Ed Schneider, Melvin Hagge, Steve Chacko, Dan Stiurca

Crystal - Cirrus Logic Inc. Austin TX

A low-jitter frequency synthesizer in 0.18µm CMOS uses the sample-reset loop filter technique to achieve a process-independent damping factor and low jitter operation with minimum ripple-filtering pole requirements. PLL specifications include: operating range 125-1250MHz, resolution <500kHz, jitter <0.3%?Tosc, and power dissipation 75mW from 2.5V supply.

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L. Wu

25.3: A Low-Jitter Skew-Calibrated Multi-Phase Clock Generator for Time-Interleaved Applications

Lin Wu, William C. Black Jr.

Iowa State University, Ames, IA

An adaptive skew-compensating four-phase clock generator operating from 100MHz-250MHz continuously self-calibrates skew of the output clocks. Pre-calibration edge timing skews of 50ps or more are automatically reduced to <10ps in 0.25µm standard bulk CMOS process operating at 2.5V.

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K. Yamaguchi

25.4: A 2.5GHz 4-phase Clock Generator with Scalable and No Feedback Loop Architecture

Kouichi Yamguchi, Muneo Fukaishi, Takehiko Sakamoto, Naoto Akiyama, and Kazuyuki Nakamura

NEC Corp., Sagamihara, Kanagawa, Japan

An accurate simple multi-phase clock generator using delay compensation based on phase interpolation is applied to 2.5GHz 4-phase clock distribution of a 5Gb/s x 8-channel receiver in 0.13µm CMOS technology. The 4-phase generator in the receiver consumes 30mW and occupies 0.009mm^2.

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J. Wood

25.5: Multi-GHz Low-Power Low-Skew Rotary Clock Scheme

John Wood[1], Steve Lipa[2], Paul Franzon[2], Michael Steer[2]

[1]Multigig Corporation Ltd., [2]North Carolina State University

A clock distribution scheme for VLSI circuits uses rings of differential lines driven by inverter pairs to distribute a low-skew low-jitter clock over an arbitrarily large die area with low power consumption. Results are shown for a prototype with 950MHz and 3.42GHz rings.

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T. Xanthopoulos

25.6: The Design and Analysis of the Clock Distribution Network for a 1.2GHz Alpha Microprocessor

Thucydides Xanthopoulos, Daniel W. Bailey, Atul K. Gangwar, Michael K. Gowan, Anil K. Jain, Brian K. Prewitt

Compaq Computer Corp., Shrewsbury, MA

A 1.2GHz clock system for a 0.18µm CMOS microprocessor employs three digital DLLs to phase-lock the memory and interface clocks to the core CPU clock. The fully-digital DLLs use a 64/8 coarse/fine delay line to extend the locking range.

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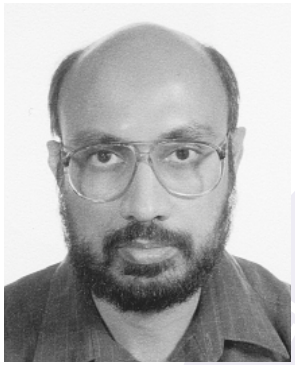

J. Barkatullah

25.7: A Multi-GHz Clocking Scheme for Pentium® 4 Microprocessor

Nasser A. Kurd, Javed S. Barkatullah, Rommel O. Dizon, Thomas D. Fletcher, Paul D. Madland

Intel Corp., Hillsboro, OR

Two tightly-synchronized PLLs generate core and IO clocks on this 4th generation IA32 microprocessor. Clock distribution to 47 domains is adjusted for supply, loading, and on-die variations to reduce skew to 20ps. Pulse and double frequency clocks are locally generated.

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R. Magoon

26.1: A Triple-Band 900/1800/1900MHz Low-Power Image-Reject Front-End For GSM

Rahul Magoon[1], Iconomos Koullias[2], Luke Steigerwald[2], William Domino[1], Nooshin Vakilian[1], Emmanuel Ngompe[1], Morten Damgaard[1], Kevin Lewis[2], Alyosha Molnar[1]

[1]Conexant Systems Inc., Newport Beach CA
[2]Wireless Microsystems, Reading, PA

A triple-band RF front-end including on-chip integrated LC image-reject filters achieves >40dB image rejection over all bands with 15-18mA supply current. The device uses 28 on-chip spiral inductors on a 2.25x2.75mm^2 BiCMOS die. Measured NF is 2.5dB(GSM), 3.6dB(DCS), 3.8dB(PCS) and measured input 1dB compression is >-21dBm.

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P. Leroux

26.2: A 0.8dB NF ESD-Protected 9mW CMOS LNA

Paul Leroux, Johan Janssens and Michiel Steyaert

Katholieke Universiteit Leuven, Leuven, Belgium

A 0.25µm CMOS LNA for the L2 GPS band at 1.2276GHz features 0.8dB noise figure and 20dB power gain consuming 9mW. Apart from the input bonding wire, the 50Ω input and output matching networks are implemented on-chip. The ESD-protection at the input withstands HBM-pulses from -1.4 to 0.6kV.

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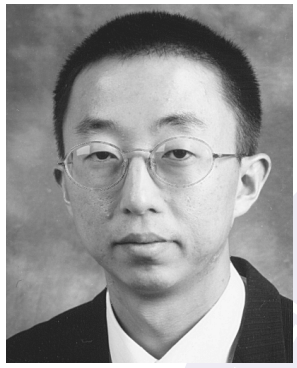

H. Wu

26.3: A 19GHz 0.5mW 0.35µm CMOS Frequency Divider with Shunt-Peaking Locking-Range Enhancement

Hui Wu and Ali Hajimiri

California Institute of Technology, Pasadena, CA

Shunt-peaking locking-range enhancement used in a 19GHz 0.35µm CMOS injection-locked frequency divider (ILFD) gives 760MHz locking range and 0.5mW dissipation at -12dBm injection power level. The locking range can be further increased with higher injection power. A second 9GHz ILFD with 880MHz locking range is also reported.

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O. Watanabe

26.4: A 2GHz Down-Converter with 600MHz 3dB Bandwidth using LO Signal Suppressing Output Buffer

Osamu Watanabe, Takafumi Yamaji, Tetsuro Itakura, Ichiro Hattori

Toshiba Corp., Kawasaki, Japan

A 2GHz down-converter with a 3dB bandwidth of 600MHz is fabricated in BiCMOS process. The conversion gain varies <0.7dB for temperature range from -34 to 85°C. NF is 9.5dB and IIP3 is -5dBm. The down-converter consumes 15mA from 2.7V power supply, and occupies approximately 1mm^2.

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J. Lin

26.5: 3V GSM Base Station RF Receivers using 0.25µm BiCMOS

Jenshan Lin, Olga Boric-Lubecke, Penny Gould[1], Chris Zelley[2], Yung-Jinn Chen[3], and Ran-Hong Yan

Bell Laboratories, Lucent Technologies, Murray Hill, NJ, [1] Swindon, UK, [2]DERA, Worcestershire, UK, [3]WIN Semiconductors, Taiwan

Two integrated RF receivers for GSM900 and DCS1800 base stations use a 0.25µm BiCMOS process. Noise figure, gain, and output IP3 are 2.1dB, 25.3dB, and 23.6dBm for GSM900, and 3.3dB, 20.7dB, 21.6dBm for DCS1800, respectively.

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A. Zolfaghari

26.6: A 2.4GHz 34mW CMOS Transceiver for Frequency-Hopping and Direct-Sequence Applications

Alireza Zolfaghari, Andrew Chan, Behzad Razavi

Electrical Engineering Department,
University of California, Los Angeles, CA

A 2.4GHz heterodyne transceiver consists of a dual-downconversion receiver with partial channel-selection filtering, a two-step quadrature upconversion transmitter, and a 1.6GHz frequency synthesizer. Fabricated in a 0.25µm CMOS technology, the transceiver consumes 34mW.

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R. Hofmann

26.7: SiGe BiCMOS Broadband Phase Aligner from 1 to 11Gb/s

Ralf Hofmann, Bjoern Jelonnek, Helmut Kling, Armin Splett, Eric Koenig

Siemens AG, Ulm, Germany

A phase aligner for serial bit stream uses SiGe BiCMOS technology. It operates from 1 to 11Gb/s and is a complete digital architecture.

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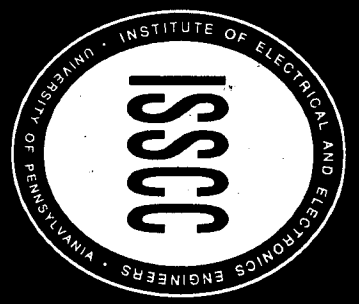

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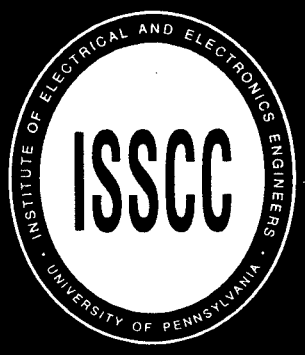

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ISSN 0193-6530

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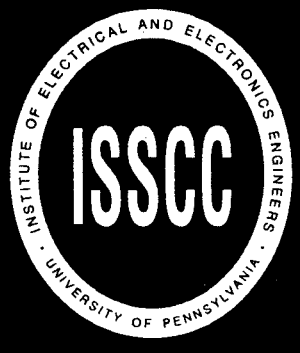
1993 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

WEDNESDAY, THURSDAY, and FRIDAY / FEBRUARY 24, 25, and 26, 1993

40th ANNIVERSARY



1993 COMMEMORATIVE SUPPLEMENT

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39th ISSCC

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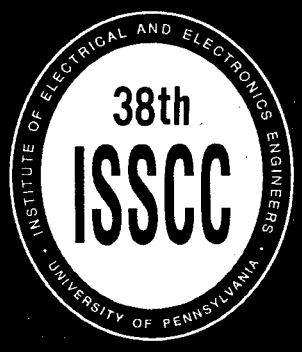
1991 IEEE INTERNATIONAL

SOLID-STATE CIRCUITS CONFERENCE



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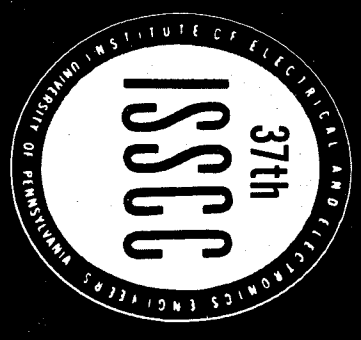

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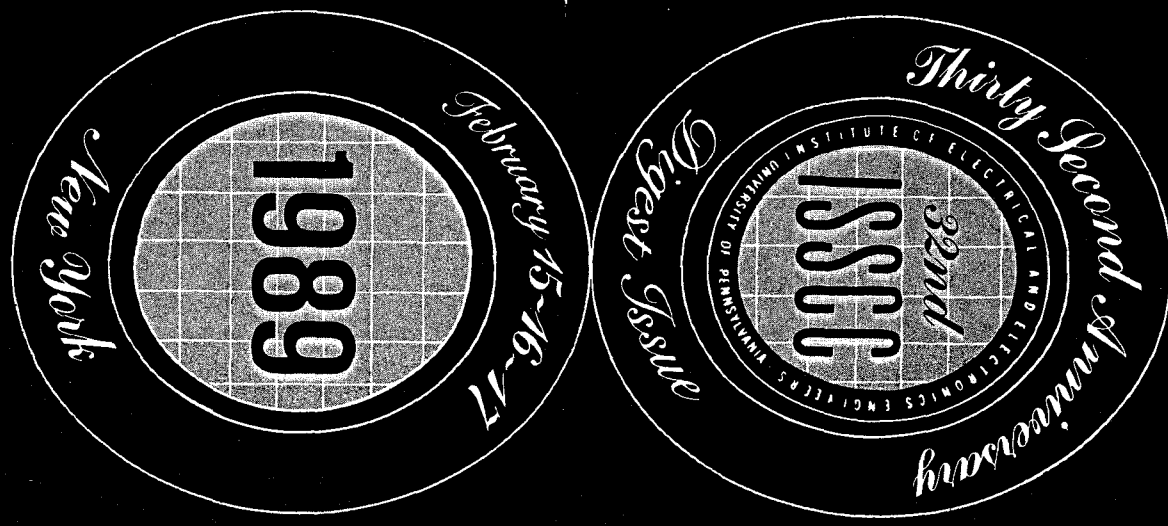

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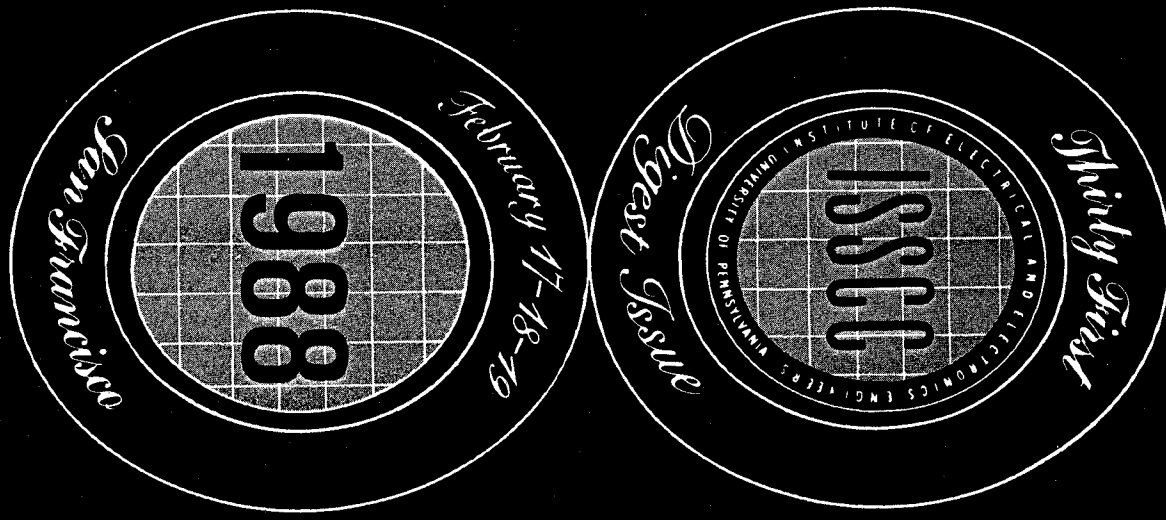

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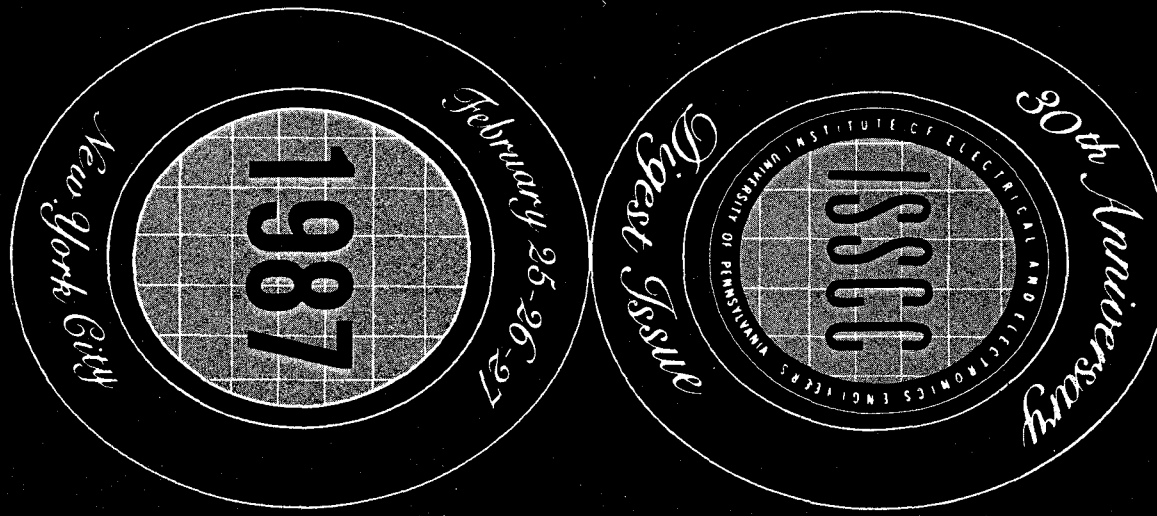

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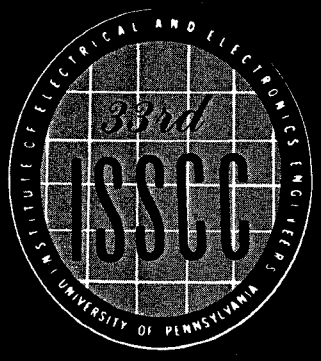

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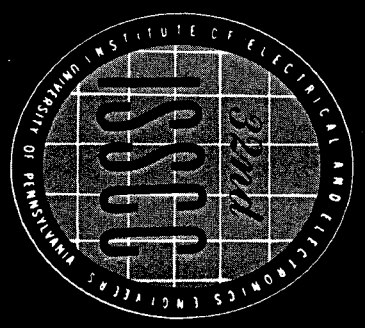

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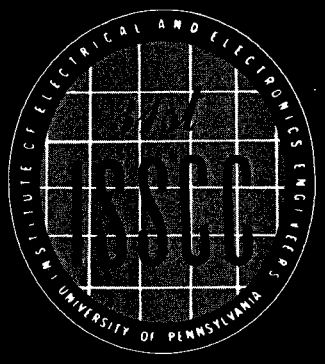

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